Pixel
Semiconductor
A Cirrus Logic Company

CL-PX2080

MediaDAC™

Advance Product Information

The CL-PX2080 MediaDAC™ is a multiple source, digital-to-analog video converter. It manages and mixes two different video data streams while converting the input data into the format of the display subsystem, and changes color space and resolution from the input to the output format in real time.

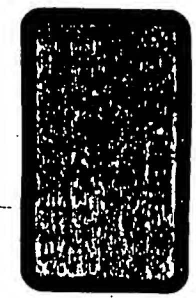
MediaDAC~

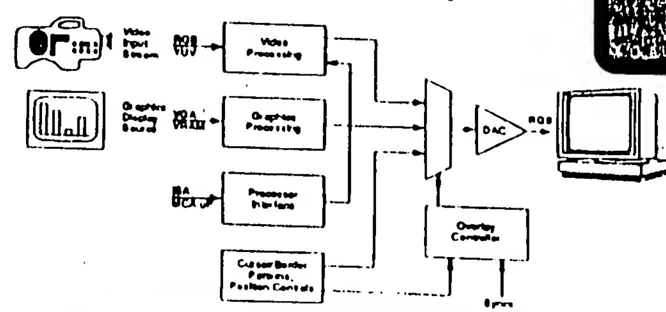
FEATURES

- Direct ISA/MCA bus interface
- Interlaced or non-interlaced output
- Up to 85 MHz pixel clock rates
- Video Inputs
  - 8:8:8 RGB at 40 MHz
  - 1:5:5:5 (T)RGB at 85 MHz
  - 5:6:5 RGB
  - 4:2:2 YUV at 85 MHz
  - tagged 4:2:2 YUV at 85 MHz
- Zoom controls
- Hardware cursor controls
- Three overlay combination controls
  - tagged chroma color key
  - graphics overlay color key
  - X/Y window
- Graphics Input
  - 4 bit pseudocolor at 85 MHz
  - 8 bit pseudocolor at 85 MHz
  - 5:5:5 RGB at 85 MHz
  - 5:6:5 RGB at 85 MHz
  - 8:8:8 RGB at 40 MHz

APPLICATIONS

- Presentation
- Video Editing
- Video Authoring
- Video Teleconferencing
- Interactive Education
- Games





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September, 1992

DEPOSITION EXHIBIT Shafer 10

YUV
# # #

what is YUV + # # # ?
for RGB # # # RGB ?

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ARCHITECTURAL OVERVIEW

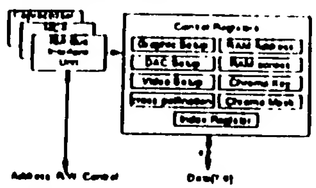
This section describes the architecture and functionality of the CL-PX2080 MediaDAC™.

The CL-PX2080 has a video port for YCbCr or RGB data and a graphics port with both 8 bit VGA and 32 bit high resolution ports. Its display functions include:

- pseudocolor,
- display of true color RGB data,
- X zooming,
- hardware cursor controls, and
- a combination of three graphics overlay controls

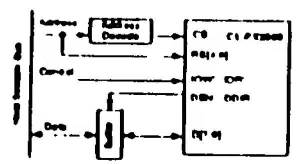
Host System Interface

The CL-PX2080 connects directly to ISA and MCA buses, internally decoding a 16 bit address and responding as an 8 bit peripheral. Its internal ISA/MCA bus interface eliminates most of the costly "glue" circuitry common to many personal computer system expansion boards.



In response to customer demands for increased performance, the display subsystem in many new systems has migrated onto the host processor bus. The CL-PX2080 is designed to accommodate

this trend with its local hardware interface mode, if ... here



Video Input Interface

The video input interface accepts digitized video in a wide range of formats. The video data stream is converted to its final output format, then is mixed and/or overlaid with processed graphics data and cursor data.

Features:

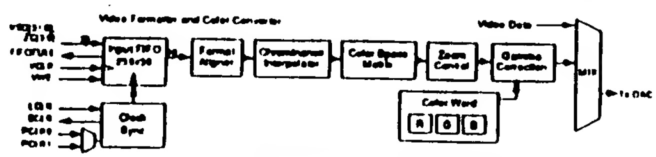
- 36 bit input data path,
- Internal 256×36 bit input FIFO that supports
  - 24 bit RGB data (up to 40 mega pixels)
  - 16 bit RGB or YCbCr data (up to 85 mega pixels)
- chrominance format alignment,
- color space interpolation,
- zoom control

Graphics Frame Buffer Interface

The CL-PX2080 accepts data from the graphics display source through either of two paths

- an 8 bit VGA data path, or
- a 32 bit VRAM serial data path

Both paths allow CL-PX2080 based, next generation PC graphics subsystems to maintain compati-



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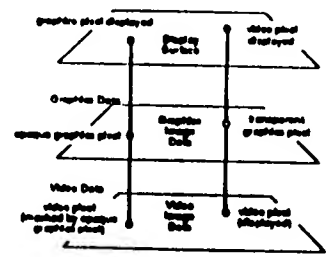
- designed to accept data from VRAM serial ports, can be used with a variety of architectures
- VGA interface
- true color (CLUT bypass) option

Graphics Overlay Control

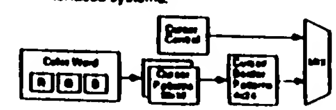
The graphics overlay controls allow a video image and a graphics image to be combined using a variety of operations (see figure right)

Every graphics pixel is either transparent or opaque. The color information for an opaque pixel is displayed on the screen. The color information for a transparent pixel is not displayed; instead, the color information of the video pixel behind it is displayed on the screen. The graphics overlay controls determine which graphics pixels are transparent. The CL-PX2080 has 256 possible overlay combinations based on the video pixel tag bit, the graphics pixel overlay color, and the XY window of the video data.



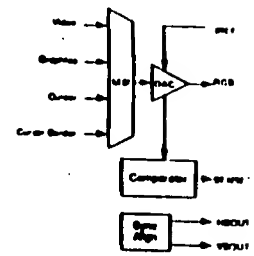
Cursor

The CL-PX2080 implements an on-chip, three-color, user-definable hardware cursor in a 32x32x2 bit memory. This cursor works in both interlaced and non-interlaced systems.



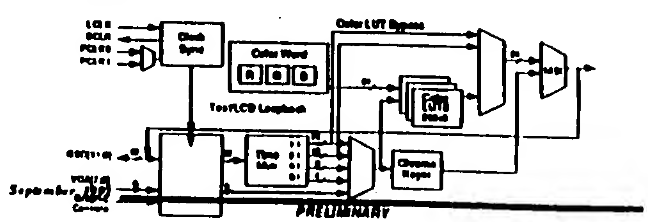
Output DACs

The CL-PX2080 has three video speed, 8 bit digital-to-analog converters, internal comparators to provide the sense function, and sync alignment logic. These form a complete RGB monitor interface.



Power Down Mode

During the CL-PX2080's power-down condition, the DACs power down and the RAM enters a low-power, data-retaining standby mode. The proces



[illegible] can read from or write to the RAM as long as the pixel clock is running. The RAM automatically powers up during processor read/write cycles and shuts down when processor access is complete. The three DAC command registers are also accessible.

SOFTWARE SUPPORT

Pixel Semiconductor provides a complete solution for computer based video. Multilevel software support is available to ensure a quick product development cycle that keeps up with today's fast time to market requirements.

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The Company

Cirrus Logic, Inc., is a leading supplier of high integration peripheral controller circuits for mass storage, graphics, and data communications. The company also produces state-of-the-art software and firmware to complement its product lines. Cirrus Logic technology is used in leading-edge personal computers, engineering workstations, and office automation.

Pixel Semiconductor, Inc., a subsidiary of Cirrus Logic, Inc., is a developer of integrated circuits for advanced display systems. These circuits enable the integration of real-time video with traditional computer graphics.

Cirrus Logic's extensive quality assurance program — one of the industry's most stringent — ensures the utmost in product reliability. Talk to our systems and applications specialists; see how you can benefit from a new kind of semiconductor company — Cirrus Logic.

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September, 1992

May 1991

Table of Contents

Cirrus Confidential
Business Information

CL 41986

List of Figures

CL 41988

Cirrus Confidential Business Information

List of Tables

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Business Information

CL 41989

1. PIN INFORMATION

The CL-PX2080 MediaDAC™ is available in a 160-pin Plastic Quad Flat Pack (PQFP) device that can be configured for ISA, MCA or Coprocessor bus implementation.

1.1 Pin Diagrams

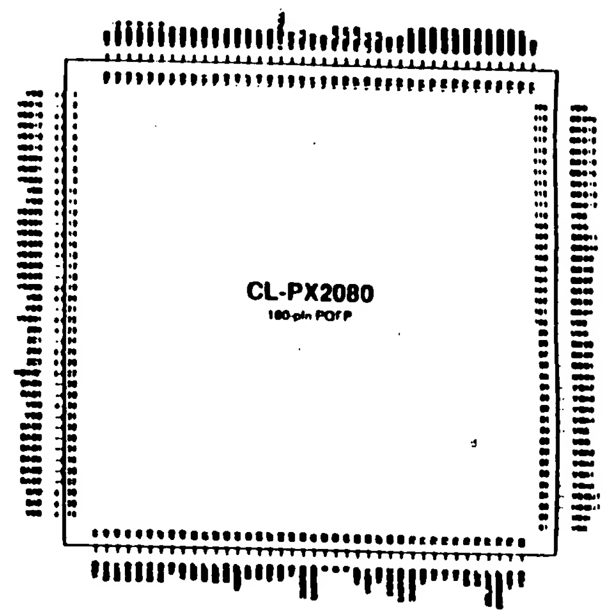

Figure 1-1. Pin Diagram — ISA Bus Configuration

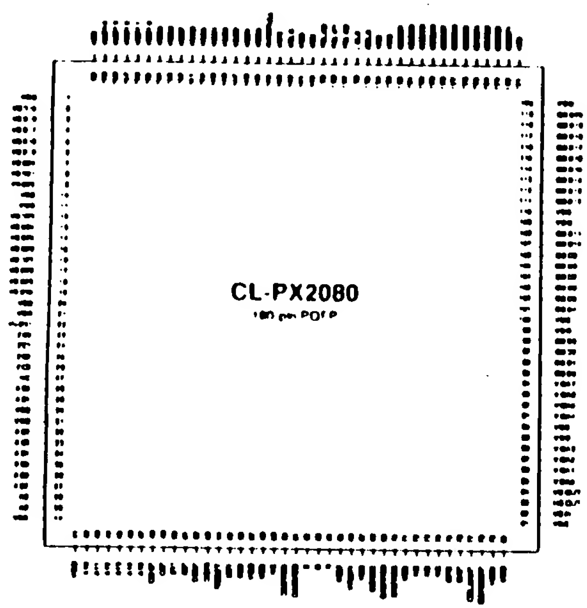

Figure 1-2. Pin Diagram — MCA Bus Configuration

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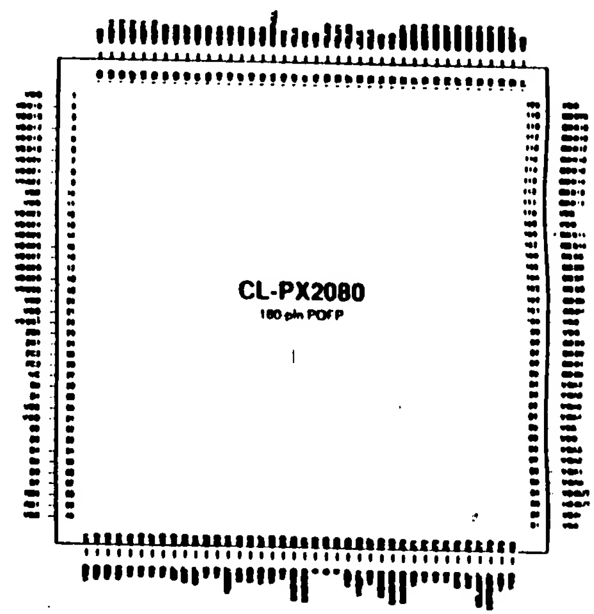

Figure 1-3. Pin Diagram — Coprocessor Bus Configuration

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1.2 Pin Assignment Table

The following conventions are used in the pin assignment table:

- * = negative true signal
- I = input
- O = output
- AN = analog signal
- PU = internal pull up
- PWR = power
- TTL = the pad has standard TTL input threshold and TTL output levels
- CMOS = the pad has standard CMOS input threshold and CMOS output levels
- 3S = three state TTL drive capability
- OD = open drain, TTL inputs
- 4 = 4 mA sink and 2 mA source drive capability
- 12 = 12 mA sink and 4 mA source drive capability
- 24 = 24 mA sink and 8 mA source drive capability

NAME	PIN	TYPE	CELL	FUNCTION
PROCESSOR INTERFACE — ISA BUS MODE SUMMARY				
SA[15:8]	47:42, 39:38	I	TTL	CPU Address High Byte
SAD[7:0]	37:32, 29:28	I/O	3S, 12	CPU Address and Data Low Byte
IOR*	80	I	TTL	I/O Read
IOW*	81	I	TTL	I/O Write
AEN	49	I	TTL	Address Enable
RESET	84	I	TTL	Reset
NOWS*	27	O	OD, TTL, 24	No Wait State
DEN*	52	O	TTL, 8	Data Buffer Enable
DDIR	53	O	TTL, 8	Data Buffer Direction
BS[1:0]	85 56	I	TTL	Bus Select
ALT	89	I	TTL	BIR alternate address select
NC	48	N/A	N/A	No Connect (must be left floating)
PROCESSOR INTERFACE — MCA BUS MODE SUMMARY				
A[15:8]	47:42, 39:38	I	TTL	CPU Address High Byte
AD[7:0]	37:32, 29:28	I/O	3S, 12	CPU Address and Data Low Byte
NC	27	N/A	N/A	No Connect (must be left floating)
CMD*	49	I	TTL	Command
M/IO*	48	I	TTL	Memory or I/O Cycle
S1*	80	I	TTL	Status 1
S0*	81	I	TTL	Status 0
CDRESET	84	I	TTL	Reset
DEN*	82	O	OD, TTL, 8	Data Buffer Enable
DDIR	83	O	OD, TTL, 8	Data Buffer Direction
BS[1:0]	85 56	I	TTL	Bus Select
ALT	89	I	TTL	BIR alternate address select

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May 1991

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NAME	PIN	TYPE	CELL	FUNCTION
PROCESSOR INTERFACE — COPROCESSOR BUS MODE SUMMARY				
RS[4:0]	44:42, 39:38	I	TTL	Register Select
D[7:0]	37:32, 29:28	I/O	3S, 12	Data
IOR*	80	I	TTL	I/O Read Cycle
IOW*	81	I	TTL	I/O Write Cycle
RESET	84	I	TTL	Reset
CS*	49	I	TTL	Chip Select
BS[1:0]	85 86	I	TTL	Bus Select
NC	53 52	N/A	N/A	No Connect (must be left floating)
NC	48	N/A	N/A	No Connect (must be left floating)
NC	47 45	N/A	N/A	No Connect (must be left floating)
NC	27	N/A	N/A	No Connect (must be left floating)
GRAPHICS PORT INTERFACE				
GSD[31:0]	132:122, 119:111, 108:101, 98:95	I/O	3S, 8	Graphics Source Data
VGA[7:0]	94:91, 88:85	I	TTL	VGA Graphics Source Data
PCLK0	139	I	TTL	Pixel Input Clock 0
PCLK1	138	I	TTL	Pixel Input Clock 1
LCLK	136	I	TTL	Latch Clock Input
SCLK	135	O	TTL, 12	VRAM Shift Clock Output
O/E*	70	I	TTL	Odd/Even Field Input
GPS	76	I	TTL	Graphics Port Select
BORDER*	78	I	TTL	Active Display Border
CBLANK*	77	I	TTL	Composite Blank Input
VSIN	82	I	TTL	Vertical Sync Input
HSIN	79	I	TTL	Horizontal Sync Input
VSOUT	84	O	TTL, 8	Vertical Sync Output
HSOUT	83	O	TTL, 8	Horizontal Sync Output
PCLK2	137	O	TTL, 12	Pixel Clock Output
VIDEO PORT INTERFACE				
VSD[31:0]	22, 18:12, 92, 180:148	I	TTL	Video Source Data
ZC[3:0]	20:23	I	TTL	Zoom Control Code
FIFOFULL	144	O	TTL, 8	FIFO Full Indication
VCLK	142	I	TTL	Video Clock Input
VWE	143	I	TTL	Video FIFO Write Enable

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NAME	PIN	TYPE	CELL	FUNCTION
MONITOR INTERFACE				
R	84	O	AN	Analog Red
G	83	O	AN	Analog Green
B	82	O	AN	Analog Blue
IREF	85	I	AN	Current Reference
SENSE	88	O	TTL, 8	Monitor Sense
VREF1	86	O	AN	Voltage Reference 1
POWER INTERFACE				
VDD	1, 11, 21, 31, 41, 57, 80, 89, 99, 109, 120, 131, 141	PWR		+5 VDC for Digital Logic and Interface Buffers
VSS	10, 20, 30, 40, 58, 67, 71, 81, 90, 100, 110, 121, 134, 140, 160	PWR		Ground for Digital Logic and Interface Buffers
DACVDD	61, 69	PWR		+5 VDC for DAC
DACVSS	60, 70	PWR		Ground for DAC
NO CONNECTS				
NC	72	N/A	N/A	No Connect (must be left floating)
NC	73	N/A	N/A	No Connect (must be left floating)
NC	74	N/A	N/A	No Connect (must be left floating)

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2. DETAILED SIGNAL DESCRIPTION

2.1 Processor Interface - ISA Bus Mode

Signal	Pin	Type	Cell	Function
SA[15:8]	47-42, 39:38	I	TTL	**CPU Address High Byte:** SA[15:8] specify the resource to be accessed during an I/O or memory cycle.
BAD[7:0]	37:32, 29:28	I/O	3S, 12	**CPU Address and Data Low Byte:** The lower byte of address is multiplexed with low byte of data externally to transfer data to and from the CL-PX2080 during an I/O cycle.
IOR*	50	I	TTL	**I/O Read:** This active low input signal indicates an I/O read cycle
IOW*	51	I	TTL	**I/O Write:** This active low input signal indicates an I/O write cycle
AEN	49	I	TTL	**Address Enable:** This active high input signal indicates a DMA cycle is in progress.
RESET	54	I	TTL	**Reset:** This active high input signal indicates that the CL-PX2080 is to cease all activity and perform a hardware reset
NOWS*	27	O	OD, TTL, 24	**No Wait State:** This open drain output specifies that the host should run a zero wait state cycle. The default ISA bus cycle is one wait state
DEN*	62	O	TTL, 8	**Data Buffer Enable:** This open drain output, when pulled low, enables the host data bus buffer.
DDIR	63	O	TTL, 8	**Data Buffer Direction:** This open drain output specifies the direction of data flow on bus BAD[15:0]. A high level indicates that the host system is driving data to BAD[15:0] (write cycle), and a low level indicates that the CL-PX2080 is driving BAD[15:0] (read cycle) to the host system.
BS[1:0]	55:56	I	TTL	**Bus Select:** These two bits indicate the bus mode selected for the operation of the CL-PX2080. 0 0 ISA bus mode 0 1 MCA bus mode 1 0 Local hardware interface mode
ALT	50	I	TTL	**Alternate address select:** Enables secondary ISA address range for BIR access. 0 Primary ISA address range 1 Secondary ISA address range
NC	48	N/A	N/A	**No Connect** (must be left floating)

2.2 Processor Interface - MCA Bus Mode

Signal	Pin	Type	Cell	Function
A[15:8]	47 42 39 38	I	TTL	CPU Address High Byte: A[15:8] specifies the resource to be accessed during an I/O or memory cycle
AD[7:0]	37 32 29 28	I/O	35, 12	CPU Address and Data Low Byte: AD[7:0] is multiplexed with data externally to transfer data to and from the CL-PX2080 during an I/O cycle
NC	27	N/A	N/A	No Connect (must be left floating)
CMD'	48	I	TTL	Command: This active low input signal indicates valid data is on bus AD[15:0] during a write cycle, and that the CL-PX2080 should place valid data on the bus during a read cycle
M/IO'	49	I	TTL	Memory or I/O Cycle: This active low signal works with S1' and S0' to specify the current bus cycle M/IO' S0' S1' 0 0 0 Reserved 0 0 1 I/O Write 0 1 0 I/O Read 0 1 1 Inactive 1 0 0 Reserved 1 0 1 Memory Write 1 1 0 Memory Read 1 1 1 Inactive
S1'	50	I	TTL	Status 1: This active low signal works with M/IO' and S0' to specify the current bus cycle (see table under M/IO')
S0'	61	I	TTL	Status 0: This active low signal works with M/IO' and S1' to specify the current bus cycle (see table under M/IO')
CDRESET	64	I	TTL	Reset: This active high input signal indicates that the CL-PX2080 is to cease all activity and perform a hardware reset.
DEN'	52	O	OD, TTL, 8	Data Buffer Enable: This open drain output, when pulled low, enables the host data bus buffer.
DDIR	53	O	OD, TTL, 8	Data Buffer Direction: Indicates the direction of data flow on bus SAD[15:0]. A high level indicates that the host system is driving data to SAD[15:0] (write cycle), and a low level indicates that the CL-PX2080 is driving SAD[15:0] (read cycle) to the host system
BS[1:0]	55 56	I	TTL	Bus Select: These two bits indicate the bus mode selected for the operation of the CL-PX2080 0 0 ISA bus mode 0 1 MCA bus mode 1 0 Local hardware interface mode

CL 41994

21

May 1991

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Signal	Pin	Type	Cell	Function
ALT	80	I	TTL	Alternate address select: Enables secondary ISA address range for BIR access. 0 Primary ISA address range 1 Secondary ISA address range

2.3 Processor Interface - Coprocessor Bus Mode

Signal	Pin	Type	Cell	Function
RS[4:0]	44 42, 39 38	I	TTL	Register Select: RS[4:0] specify the internal register to be accessed during a CL-PX2080 I/O cycle.
D[7:0]	37 32, 29 28	I/O	35, 12	Data: D[7:0] is an active high bidirectional data bus used to access the internal control registers.
IOR'	60	I	TTL	I/O Read Cycle: This active low input signal indicates an I/O read cycle
IOW'	61	I	TTL	I/O Write Cycle: This active low input signal indicates an I/O read cycle.
RESET	64	I	TTL	Reset: This active high input signal indicates that the CL-PX2080 is to cease all activity and perform a hardware reset
CS'	49	I	TTL	Chip Select: This active low input indicates that the CL-PX2080 is being accessed by the host system.
BS[1:0]	55 56	I	TTL	Bus Select: These two bits indicate the bus mode selected for the operation of the CL-PX2080. 0 0 ISA bus mode 0 1 MCA bus mode 1 0 Local hardware interface mode
NC	63 52	N/A	N/A	No Connect (must be left floating)
NC	48	N/A	N/A	No Connect (must be left floating)
NC	47 46	N/A	N/A	No Connect (must be left floating)
NC	27	N/A	N/A	No Connect (must be left floating)

2.4 Graphics Port Interface

Signal	Pin	Type	Cell	Function
OSD[31:0]	132-127 119-111 98-101 88-95	I/O	15, 8	Graphics Source Data: OSD[31:0] is selected when GPS = 1. OSD[31:0] is a 32 bit VRAM serial data path that inputs data at 4, 8 and 16 bits per pixel. GPS selects either the VGA source or the OSD source into the graphical data path. OSD[31:0] is latched on the rising edge of LCLK. All unused bits must be connected to VSS. When CSC register bits (8,5) = 11, the OSD signals are mapped to the DAC inputs as follows: OSD[23:16] to R[7:0] OSD[15:8] to G[7:0] OSD[7:0] to B[7:0] (This is primarily a test mode feature, but may input to LCD control for. This output mode will not run at maximum frequency.)
VGA[7:0]	84-81 88-85	I	TTL	VGA Graphics Source Data: VGA[7:0] is selected when GPS = 0. VGA[7:0] is latched on the rising edge of LCLK. All unused bits must be connected to VSS.
PCLK0	139	I	TTL	Pixel Input Clock 0: PCLK0 is the VGA input clock. It is selected when Bit 4 of the CSC register = 0.
PCLK1	138	I	TTL	Pixel Input Clock 1: PCLK1 is the high speed OSD[31:0] input clock used during multiplexed operation of the 32 bit VRAM serial pixel port. It is selected when Bit 4 of the CSC register = 1.
LCLK	136	I	TTL	Latch Clock Input: The rising edge of LCLK latches OSD[31:0] or VGA[7:0] and BLANK*, HSIN, VSIN, GPS and BORDER*, which are then synchronized internally with SCLK. To avoid metastability LCLK must maintain setup and hold requirements to SCLK. Data is synchronized with PCLKn after being internally latched with SCLK. When the input data multiplexing ratio is 8:1, 4:1, 2:1, or 1:1, LCLK must equal PCLKn divided by 8, 4, 2, or 1, respectively.
SCLK	135	O	TTL, 12	VRAM Shift Clock Output: SCLK = PCLKn divided by 8, 4, 2 or 1, depending on the operating mode specified.
O/E*	78	I	TTL	Odd/Even Field Input: The cursor controller uses O/E* to insure proper operation in interlaced mode, and ignores it in non interlaced mode. O/E* should be changed only during vertical blanking.
GPS	75	I	TTL	Graphics Port Select: When GPS is asserted high and bits (8,5) of the CSC register are 1, OSD[31:0] becomes the graphic port. When GPS is asserted low and bits (8,5) of the CSC register are 1, VGA[7:0] becomes the graphics port. GPS is disabled when bits (8,5) of the CSC register are not 1.

CL 41995

23

May 1991

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Signal	Pin	Type	Cell	Function
BORDER*	78	I	TTL	Active Display Border: BORDER*, BLANK*, and GPS specify whether the DAC outputs are blanked or contain cursor, pixel or border color, as shown below. BORDER* = 1 when a display border is not used. BLANK* BORDER* GPS 0 X X Video blanking 1 0 X Border color 1 1 0 VGA or cursor color 1 1 1 OSD or cursor color.
CBLANK*	77	I	TTL	Composite Blank Input: CBLANK* applies a color value of 0 to the DAC inputs to produce black at the DAC outputs. The cursor position counters are referenced to CBLANK*.
VSIN	82	I	TTL	Vertical Sync Input: VSIN generates a vertical sync pulse once every frame in non-interlaced mode, and once every field in interlaced mode. VSIN is polarity programmable.
HSIN	79	I	TTL	Horizontal Sync Input: HSIN generates a horizontal sync pulse every line. HSIN is polarity programmable.
VSOUT	84	O	TTL, 8	Vertical Sync Output: VSOUT is a polarity programmable delay of HSIN.
HSOUT	83	O	TTL, 8	Horizontal Sync Output: HSOUT is a polarity programmable delay of HSIN or a composite SYNC generated from HSIN and VSIN, as determined by the SAR register.
PCLK2	137	O	TTL, 12	Pixel Clock Output:

2.5 Video Port Interface

Signal	Pin	Type	Cell	Function
VSD[31:0]	22, 10-12, 92, 139-145	I	TTL	**Video Source Data:** Video data inputs to the CL-PX2080 through VSD[31:0]. The CL-PX2080 supports the following formats in both tagged and untagged modes: 16 bit YUV (4:2:2), 16 bit RGB (5:6:5), 24 bit RGB (8:8:8). VCLK transfers 16 bit modes as 2 pixels per pixel word.
ZC[3:0]	20-23	I	TTL	**Zoom Control Code:** ZC[3:0] specify several options for interpolation and alignment of the input video stream on VSD[31:0] (when used with CL-PX2070).
FIFOFULL	144	O	TTL, 8	**FIFO Full Indication:** FIFOFULL* is asserted low when a full condition occurs in the 256 deep double-pixel FIFO, to indicate to the external video source that the FIFO is nearly full.
VCLK	142	I	TTL	**Video Clock Input:** On its rising edge, VCLK clocks VSD[31:0] and ZC[3:0] data into the CL-PX2080 input video FIFO if VWE is high. VCLK is generated by the source video processor.
VWE	143	I	TTL	**Video FIFO Write Enable:** If VWE is asserted high, data is written on the rising edge of VCLK. If VWE is asserted low, writes are disabled.

2.6 Monitor Interface

Signal	Pin	Type	Cell	Function
R	84	O	AN	**Analog Red:** R is the analog red channel from the 8 bit digital-to-analog converter.
G	83	O	AN	**Analog Green:** G is the analog green channel from the 8 bit digital-to-analog converter.
B	82	O	AN	**Analog Blue:** B is the analog blue channel from the 8 bit digital-to-analog converter.
IREF	85	I	AN	**Current Reference:** IREF is the required 8.8 mA reference current for the DAC.
SENSE	88	O	TTL, 8	**Monitor Sense:** Three level-detecting comparators individually monitor the red, green, and blue DAC outputs. A maximum analog DAC output level generates a high-level comparator output. A minimum analog level produces a low-level comparator output. SENSE is a logical OR of the comparator outputs.
VREF1	86	O	AN	**Voltage Reference 1:**

CL 41996

May 1991

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2.7 Power

Signal	Pin	Type	Cell	Function
VDD	1, 11, 21, 31, 41, 67, 80, 89, 99, 109, 120, 133, 141	PWR		**+5 VDC for Digital Logic and Interface Buffers:** Each VDD pin must be connected directly to the VDD plane.
VSS	10, 20, 30, 40, 56, 67, 71, 81, 90, 100, 110, 121, 134, 140, 160	PWR		**Ground for Digital Logic and Interface Buffers:** Each VSS pin must be connected directly to the ground plane.
DACVDD	61, 69	PWR		**+5 VDC for DAC:** DACVDD must be decoupled from digital VDD with a ferrite bead or inductor.
DACVSS	60, 70	PWR		**Ground for DAC:** DACVSS must be connected to the analog ground plane.

2.8 No Connects

Signal	Pin	Type	Cell	Function
NC	72	N/A	N/A	**No Connect (must be left floating)**
NC	73	N/A	N/A	**No Connect (must be left floating)**
NC	74	N/A	N/A	**No Connect (must be left floating)**

3. FUNCTIONAL DESCRIPTION

The CL-PX2080 MediaDAC™ is a multi-source, digital to analog video converter that can manage and mix two separate raster streams that have different color spaces and resolutions. As shown in the functional block diagram in Figure 3-1, the CL-PX2080 has three input ports:

- a video input port for YUV or RGB data, and
- two graphics input ports for 8 bit VGA or 32 bit high resolution graphics

The output to monitor can be pseudocolor or true color RGB. The video processing functions of the CL-PX2080 MediaDAC™ include:

- format alignment,
- chrominance interpolation,
- color space conversion,
- zoom, and
- gamma correction.

The CL-PX2080 MediaDAC™ also includes a hardware cursor, and a combination of three graphics overlay controls.

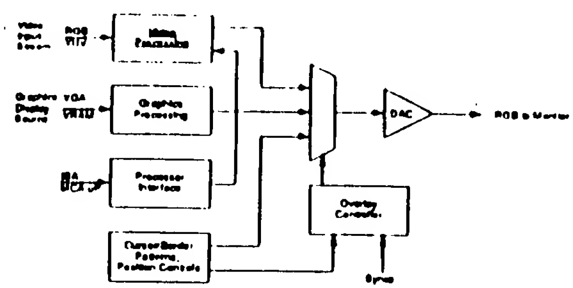

Figure 3-1. CL-PX2080MediaDAC™ Functional Block Diagram

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Figure 3-2 shows a more detailed CL-PX2080 MediaDAC™ block diagram.

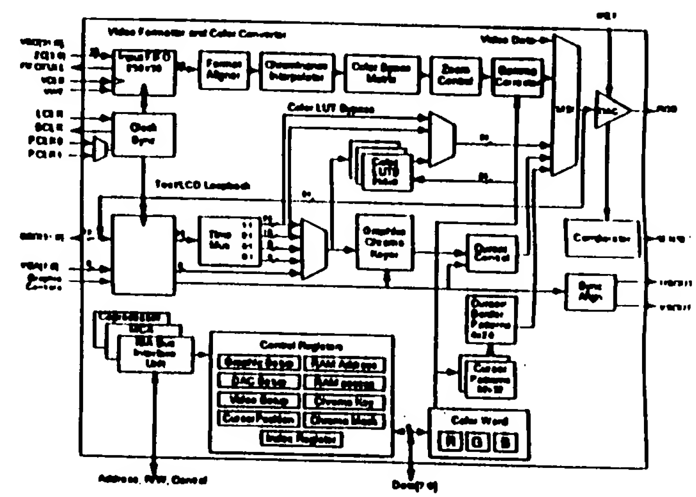

Figure 3-2. CL-PX2080MediaDAC™ Detailed Block Diagram

The primary functions of the MediaDAC™ include:

- Host Bus Interface
- Video Input Processing
- Graphics Frame Buffer Interface And Processing.

These functions are described in the following sections. For additional detail concerning specific CL-PX2080 registers, refer to Section 4.

3.1 Host Bus Interface

The CL-PX2080 interfaces with three bus protocols:

- Industry Standard Architecture (ISA) bus
- Micro Channel Architecture (MCA) bus, and
- local hardware interface.

As shown in Table 3.1 on page 29, the bus interface signals share a common set of I/O pins. For a complete pin assignment table, refer to Section 1.2 on page 17.

Table 3.1. Host System Bus I/O Pins

Pin	ISA Interface		MCA Interface		Local Hardware Interface	
27	NOWS*	O	NC	I	NC	—
[37 32 29 28]	SAD[7:0]	I/O	AD[7:0]	I/O	D[7:0]	I/O
[47 45]	SA[15:13]	I	A[15:13]	I	NC	—
[44 42 39 38]	SA[12:8]	I	A[12:8]	I	RS[4:0]	I
48	NC	—	CMD*	I	NC	—
49	AEN	I	M IO*	I	CS*	I
50	IOR*	I	S1*	I	IOR*	I
51	IOW*	I	S0*	I	IOW*	I
52	DEN*	O	DEN*	O	NC	—
53	DDIR	O	DDIR	O	NC	—
54	RESET	I	CORESET	I	RESET	I
[55 56]	BS[1:0]	I	BS[1:0]	I	BS[1:0]	I
60	ALT	I	ALT	I	NC	—

The CL-PX2080 connects directly to the ISA and MCA Buses, internally decoding a 16-bit address and responding as an 8 bit peripheral. An index and data register pair provide access to the internal registers. In local hardware interface mode, the address range is externally decoded to drive the CS* pin, with RS[4:0] selecting individual CL-PX2080 registers. Bus Selection pins BS[1:0] specify the host bus interface as shown in Table 3.2 on page 30.

Table 3-2. Bus Selection Pins

BS[1:0]	Bus Selected
00	ISA Bus
01	MCA Bus
10	Coprocessor Bus
11	Reserved

The following sections describe the configuration method for each bus.

3.1.1 ISA BUS Interface

The CL-PX2080 interfaces with an ISA bus using the pins listed in the Pin Assignment Table on page 17 to support I/O read and write cycles. Since the LSB of the address and the data pins are multiplexed, a circuit similar to that shown in Figure 3-3 is required to prevent contention between address and data buffers.

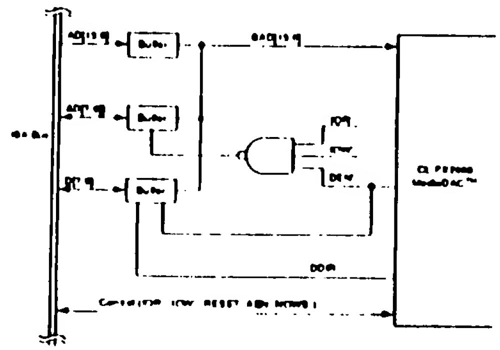

Figure 3-3 Example ISA Interface Circuit

Although the ISA bus supports both memory mapped and I/O mapped cycles, the CL-PX2080 responds only to I/O mapped bus cycles.

Figure shows a typical ISA 8 bit I/O cycle, illustrating both the similarities and differences in the read and write cycles.

The following is the sequence of events for a read cycle:

1. A valid address within the address range of the CL-PX2080 stabilizes on the address bus. The CL-PX2080 decodes the address and asserts NOWS*.
2. On the falling edge of BCLK in T2[1], the system samples NOWS* and asserts IOR*. Asserting IOR* causes the following:
   a. the CL-PX2080 latches the address on SA[15:8] and AD[7:0] on the falling edge of IOR*;
   b. the I/O buffers of AD[7:0] change from input to output mode[2];
   c. DDIR goes low, using the external buffers to output to the SD bus;

1 ISA systems have widely varying timing. Any design should include a careful analysis considering the timing specifications for the CL-PX2080. See Section 8.6.2 on page 82 for additional information.
2 The circuit should be designed to disable the low byte address buffer on IOR* assertion.

   d. DEN* is asserted, disabling the address buffers and enabling the data buffers.
3. After the appropriate time interval, the system negates IOR* and latches the data from the SD bus.
4. DDIR goes high.
5. DEN* is negated.
6. The I/O buffers of AD[7:0] change from output to input mode.
7.

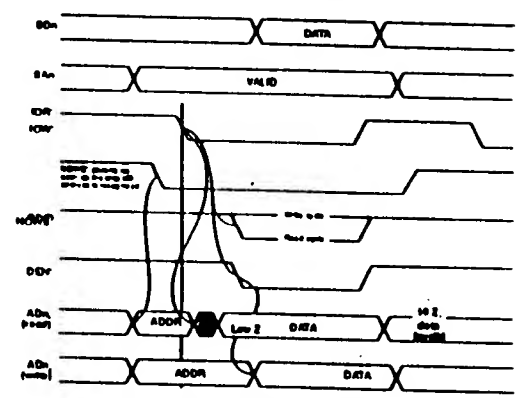

Figure 3-4. ISA 8-bit I/O Cycle

3.1.2 MCA BUS Interface

The CL-PX2080 supports I/O read and I/O write cycles for the MCA environment. The connection of the multiplexed address and data pins to the MCA bus is similar to the ISA bus connection shown in Figure 3.3 on page 31. (See Section 2.2 on page 21 for additional information.) Refer to the detailed signal description on page 21 for the MCA bus cycle decoding performed for signals M1O*, S0*, and S1*.

3.1.2.1 MCA I/O Read

Figure 3.5 shows a typical MCA 8 bit I/O cycle. The CL-PX2080 latches the address present on A[15:8] and AD[7:0] on the rising edge of ADL*. During read operations, the CL-PX2080 provides valid data on the AD[7:0] bus before the rising edge of CMD*. The CL-PX2080 outputs the data fast enough so that no wait states are required. CHRDY normally is pulled high in the MCA environment, and does not need to be driven by the CL-PX2080. Since the CL-PX2080 is an 8 bit device, the MCA environment does not require it to drive the CDDS16* signal.

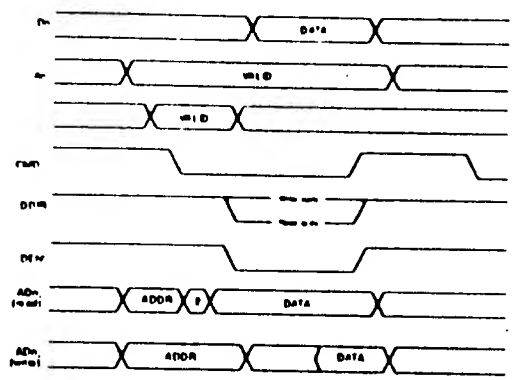

Figure 3-5. MCA 8-bit I/O Cycle

3.1.3 Local Hardware Interface

The local hardware interface is a high-speed, byte wide interface that provides the CL-PX2080 programming interface by controlling the timing of reads and writes to the CL-PX2080 in a manner similar to a static RAM. The interface has four components, which determine the read and write operations of the local hardware interface, as described in the following paragraphs:

- an 8 bit, bidirectional data bus;
- chip select input signal (CS*), which is driven by an external address decoder;
- signals RS[4:0] which select the register to be accessed, and are typically connected to the lower five

CL 42000

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bits of the processor address bus;

- control pins RD* and WR*, which define read and write cycles.

3.1.3.1 Local Access Cycles

A read from the CL-PX2080 occurs when CS* and RD* are low. Data from the addressed control register is placed on D[7:0], where it may be sampled by the host between the minimum specified access time (Section 5.5 on page 81) and the rising edge of RD*.

A write occurs when CS* and WR* are low. The host system asserts CS* after RS[4:0] are stable, then asserts WR*. Data must be valid for the specified setup and hold times relative to the rising edge of WR*. Figure 3-6 shows the timing of a local hardware access.

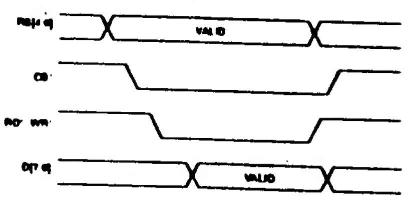

Figure 3-6. Local Hardware Interface, Cycle Timing

3.2 Video Input Processing

The video frame buffer interface has a 36 bit data bus referred to as the video port. The four most significant bits ZC[3:0] are called the data field, which is used internally by the CL-PX2080 for X zoom operations. The remaining 32 bits VSD[31:0] of the video port may contain up to eight pixels, depending on the input format control register. The CL-PX2080 supports both tagged and untagged versions of 4:2:2 YUV, 5:5:5 RGB and 8:8:8 RGB. The bitmapping of these formats onto VSD[31:0] is shown in Table 3.3 on page 36. The processing of the incoming video stream is shown in Figure 3.8 on page 36 and detailed in the sections that follow.

3.2.1 Video Input FIFO

Video port data is clocked into the CL-PX2080 independent of the graphics data. The CL-PX2080 latches video port data on the rising edge of VCLK. When the video input FIFO (full - 0) flag goes active, FIFOFULL asserts before the next VCLK rising edge. The video port data must be stable before and after the rising edge of VCLK. The video input FIFO is 256 double pixels deep.

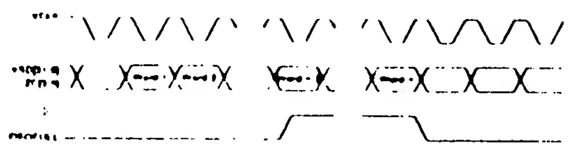

Figure 3.7. Video Input Timing

The Video Input FIFO supports 24 bit RGB color data (S 1:1 mux) at up to 40 Mhz pixel rates, 16 bit RGB (S 2:1 mux) at up to 80 Mhz pixel rates, and 16 bit YUV (S 2:1 mux) at up to 80 Mhz pixel rates. The remaining video processing elements described in this section convert a variety of input formats into linear RGB and are as follows:

- Format Aligner
- Chrominance Interpolator
- Zoom Control
- Color Space Matrix
- Gamma Corrector

These processing elements operate in sequence as shown in Figure 3-8. Any stage which is not needed for a specific application can be bypassed using internal control registers.

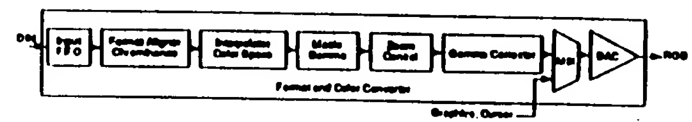

Figure 3-8. Video Input Processing Elements

3.2.2 Format Aligner

The Format Aligner accepts pixel input (VSD[31:0]) for various pixel input formats described in the table below and converts it to 4:4:4 format, 1 YUV or RGB component per pixel clock. For formats requiring less than or equal to 16 bits per pixel, 2 pixels are packed in the 32-bit pixel word, VSD[31:0]. Pipeline registers are used to reformat data before it is passed into the color conversion circuitry. The notation is based on alignment to resultant 8 bit pixel values where bit 7 is the MSb. For example, if Y 7, Y 6, Y 5, Y 4 are specified, then data is left justified out of the pipeline with the 4 LSBs padded with 0s. Also, when Y0 and Y1 are specified in the same input frame, Y0 is the first luminance component in time.

Table 3-3. Supported Pixel Word Input Formats

Pixel Word VSD[31:0]	YUV 16 bit Non-tagged	YUV 16 bit Tagged	RGB 16 bit Non-tagged	RGB 16 bit Tagged	RGB 24 bit Non-tagged	RGB 24 bit Tagged
VSD[31]	Y1-7	Y1-7	R1-7	TAG 1	X	TAG 0
VSD[30]	Y1-6	Y1-6	R1-6	R1-7	X	X
VSD[29]	Y1-5	Y1-5	R1-5	R1-6	X	X
VSD[28]	Y1-4	Y1-4	R1-4	R1-5	X	X
VSD[27]	Y1-3	Y1-3	R1-3	R1-4	X	X
VSD[26]	Y1-2	Y1-2	G1-7	R1-3	X	X
VSD[25]	Y1-1	Y1-1	G1-6	G1-7	X	X
VSD[24]	Y1-0	Y1-0	G1-5	G1-6	X	X
VSD[23]	V0-7	V0-7	G1-4	G1-5	R0-7	R0 7
VSD[22]	V0-6	V0-6	G1-3	G1-4	R0 6	R0 6
VSD[21]	V0-5	V0-5	G1-2	G1-3	R0 5	R0 5
VSD[20]	V0-4	V0-4	B1-7	B1-7	R0-4	R0 4
VSD[19]	V0 3	V0 3	B1-6	B1-6	R0 3	R0 3

Table 3-3. Supported Pixel Word Input Formats

Pixel Word VSD[31:0]	YUV 16 bit Non tagged	YUV 16 bit Tagged	RGB 16 bit Non-tagged	RGB 16 bit Tagged	RGB 24 bit Non-tagged	RGB 24 bit Tagged
VSD[18]	V0 2	V0 2	B1 5	B1 5	R0 2	R0 2
VSD[17]	V0 1	V0 1	B1 4	B1 4	R0 1	R0 1
VSD[16]	V0 0	TAG 1	B1 3	B1 3	R0 0	R0 0
VSD[15]	V0 7	V0 7	R0 7	TAG 0	G0 7	G0 7
VSD[14]	V0 6	V0 6	R0 6	R0 7	G0 6	G0 6
VSD[13]	V0 5	V0 5	R0 5	R0 6	G0 5	G0 5
VSD[12]	V0 4	V0 4	R0 4	R0 5	G0 4	G0 4
VSD[11]	V0 3	V0 3	R0 3	R0 4	G0 3	G0 3
VSD[10]	V0 2	V0 2	G0 7	R0 3	G0 2	G0 2
VSD[9]	V0 1	V0 1	G0 6	G0 7	G0 1	G0 1
VSD[8]	V0 0	V0 0	G0 5	G0 6	G0 0	G0 0
VSD[7]	U0 7	U0 7	G0 4	G0 5	B0 7	B0 7
VSD[6]	U0 6	U0 6	G0 3	G0 4	B0 6	B0 6
VSD[5]	U0 5	U0 5	G1 2	G0 3	B0 5	B0 5
VSD[4]	U0 4	U0 4	B1 7	B0 7	B0 4	B0 4
VSD[3]	U0 3	U0 3	B1 6	B0 6	B0 3	B0 3
VSD[2]	U0 2	U0 2	B1 6	B0 5	B0 2	B0 2
VSD[1]	U0 1	U0 1	B1 4	B0 4	B0 1	B0 1
VSD[0]	U0-0	TAG 0	B1 3	B0 3	B0 0	B0-0

3.2.2.1 RGB VIDEO INPUT DATA

For RGB video input data, the Format Aligner may be programmed to accept either 5-6-5, 5-5-5 TAG, 8-8-8, or 8-8-8 TAG formats, where n-n-n indicates the bits allocated to the red, green, and blue planes respectively, or pseudocolor, where the most significant input byte is passed to the red, green and blue outputs. Unused bit locations should be grounded prior to FIFO input. For RGB data, the input simply passes to the output in proper bit alignment.

CL 42002

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3.2.2.2 YUV 4:2:2 VIDEO INPUT DATA

For 4:2:2 YUV video input data, the Format Aligner can be programmed to simultaneously accept 2 pixels of data in CCIR 601 format. The Format Aligner video input formats are shown on the previous page. An optional input TAG may be used in place of the LSB of the chrominance values. Note that the chrominance values align with the odd luminance values. For 4:2:2 YUV data, the Format Aligner simply passes input data, as shown in Table 3-4 on page 38, to the Chrominance Interpolator.

Table 3-4. YUV 4:2:2 Format

Luminance Values

Y Frame	1	2	3	4	5	6	7	8
Y7	Y07	Y17	Y07	Y17	Y07	Y17	Y07	Y17
Y6	Y06	Y16	Y06	Y16	Y06	Y16	Y06	Y16
Y5	Y05	Y15	Y05	Y15	Y05	Y15	Y05	Y15
Y4	Y04	Y14	Y04	Y14	Y04	Y14	Y04	Y14
Y3	Y03	Y13	Y03	Y13	Y03	Y13	Y03	Y13
Y2	Y02	Y12	Y02	Y12	Y02	Y12	Y02	Y12
Y1	Y01	Y11	Y01	Y11	Y01	Y11	Y01	Y11
Y0	Y00	Y10	Y00	Y10	Y00	Y10	Y00	Y10

Chrominance Values

UV Frame	1		2		3		4	
UV7	U7	V7	U7	V7	U7	V7	U7	V7
UV6	U6	V6	U6	V6	U6	V6	U6	V6
UV5	U5	V5	U5	V5	U5	V5	U5	V5
UV4	U4	V4	U4	V4	U4	V4	U4	V4
UV3	U3	V3	U3	V3	U3	V3	U3	V3
UV2	U2	V2	U2	V2	U2	V2	U2	V2
UV1	U1	V1	U1	V1	U1	V1	U1	V1
UV0	U0	V0	U0	V0	U0	V0	U0	V0

3.2.2.3 YUV 4:1:1 VIDEO INPUT DATA

YUV 4:1:1 video input data is not supported at this time.

3.2.2.4 Chrominance Interpolator

The Chrominance Interpolator increases the sampling rate of the color difference signals when they are input at less than a 4:4:4 rate, and acts as a data source for the Color Space Matrix. The Chrominance Interpolator always operates in the same mode as the Format Aligner.

The Chrominance Interpolator contains two identical circuits — one for the U component and one for the V component. The output of the Time Demultiplexer feeds the Chrominance Interpolator input, setting the missing U and V values to zero on display window boundary conditions.

3.2.2.5 RGB VIDEO INPUT DATA

The Chrominance Interpolator is not required when using RGB video input data.

3.2.3 Zoom Control Codes

The Zoom Control circuitry accepts input from the Color Space Matrix and outputs to the Gamma Corrector. A 4-bit zoom code accompanies each pixel pair to specify the output sequence in the CL-PX2080 (when used with CL-PX2070).

3.2.4 Gamma Correction

The Gamma Corrector accepts input from the Color Space Matrix, and outputs to the mixing circuitry to align with incoming graphics, cursor, and background border. The Gamma Corrector can be programmed with a custom correction table, or to remove the gamma coding that is normally present in a YUV television signal.

The Gamma Corrector comprises three 256×8 memories, one for each color channel. The transfer function is user definable and programmable. A sample transfer function is supplied below. In this, the output of each circuit is its input raised to the 2.2 power (with values interpreted as fractions ranging from 0 to 255/256). The transfer function is shown in Table 3-5 on page 40.

The Gamma Corrector is an optional feature and can be bypassed by the user.

what is
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Table 3-5. Sample Gamma Removal Transfer Function

In	out	In	out	In	out	In	out	In	out	In	out	In	out	In	out
0	0	32	3	64	12	96	30	128	56	160	91	192	136	224	191
1	0	33	3	65	13	97	30	129	57	161	92	193	138	225	193
2	0	34	3	66	13	98	31	130	58	162	94	194	139	226	195
3	0	35	3	67	13	99	32	131	59	163	95	195	141	227	197
4	0	36	3	68	14	100	32	132	60	164	96	196	142	228	198
5	0	37	4	69	14	101	33	133	61	165	97	197	144	229	200
6	0	38	4	70	15	102	34	134	62	166	99	198	145	230	202
7	0	39	4	71	15	103	35	135	63	167	100	199	147	231	204
8	0	40	4	72	16	104	35	136	64	168	101	200	149	232	206
9	0	41	5	73	16	105	36	137	65	169	103	201	150	233	208
10	0	42	5	74	17	106	37	138	66	170	104	202	152	234	210
11	0	43	5	75	17	107	38	139	67	171	105	203	154	235	212
12	0	44	5	76	18	108	38	140	68	172	107	204	155	236	214
13	0	45	6	77	18	109	39	141	69	173	108	205	157	237	216
14	0	46	6	78	19	110	40	142	70	174	109	206	159	238	218
15	0	47	6	79	19	111	41	143	71	175	111	207	160	239	220
16	1	48	6	80	20	112	42	144	72	176	112	208	162	240	222
17	1	49	7	81	20	113	42	145	73	177	114	209	164	241	224
18	1	50	7	82	21	114	43	146	74	178	115	210	166	242	226
19	1	51	7	83	21	115	44	147	76	179	117	211	167	243	228
20	1	52	8	84	22	116	45	148	77	180	118	212	169	244	230
21	1	53	8	85	23	117	46	149	78	181	119	213	171	245	232
22	1	54	8	86	23	118	47	150	79	182	121	214	173	246	235
23	1	55	9	87	24	119	47	151	80	183	122	215	174	247	237
24	1	56	9	88	24	120	48	152	81	184	124	216	176	248	239
25	2	57	9	89	25	121	49	153	82	185	125	217	178	249	241
26	2	58	10	90	26	122	50	154	84	186	127	218	180	250	243
27	2	59	10	91	26	123	51	155	85	187	128	219	182	251	245
28	2	60	11	92	27	124	52	156	86	188	130	220	183	252	247
29	2	61	11	93	28	125	53	157	87	189	131	221	185	253	249
30	2	62	11	94	28	126	54	158	89	190	133	222	187	254	252
31	2	63	12	95	29	127	55	159	90	191	134	223	189	255	254

3.3 Graphics Frame Buffer Interface And Processing

The CL-PX2080 accepts data from the graphics display source through either of two paths: an 8 bit VGA data path (VGA[7:0]) or a 32 bit VRAM serial data path (GSD[31:0]). One data path is selected at a time. The GPS pin and bit 5 in the CSC register determine which input is selected. These two paths are provided to allow next generation PC graphics subsystems based on the CL-PX2080 to maintain compatibility with the large installed base of VGA systems while achieving higher performance and resolution via the VRAM serial data path.

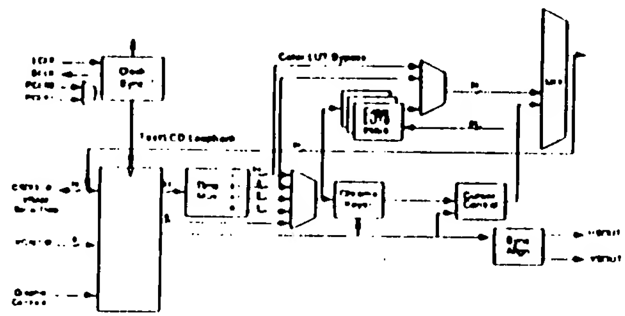

Figure 3-8. CL-PX2080 Graphics Datapath

3.3.1 VRAM Support

The graphics serial bus interface has a 32 bit data bus. The data on this bus is multiplexed under control of bits 2, 5, and 6 in the Graphics Format Control Register (GFC). Data on this bus is latched internally on the rising edge of LCLK. LCLK must be supplied by the graphics controller and should be derived from SCLK. SCLK is derived from PCLK, according to the state of bit 2 of the GFC. The maximum transfer rate on this bus is 40 Mhz (32-bit words per second).

3.3.2 VGA Support

The VGA data path is an 8 bit input bus multiplexed with the VRAM serial data path under control of bit 6 of the Graphics Setup Control Register (GSC). The maximum transfer rate is 65 Mhz (65 MBytes per second).

After the CL-PX2080 scales the video image, the resulting pixel data is stored in the FIFO. An external memory controller then transfers pixels from the FIFO to the display buffer memory, using addresses generated by an external pixel address calculator. The CL-PX2080 provides control signal outputs that simplify these operations.

CL 42004

3.3.3 VRAM Operation

3.3.3.1 Graphics Data - GSD[31:0]

The VRAM shift clock (SCLK) is generated by the CL-PX2080. In 1:1/VGA mode SCLK = LCLK. Table 3-7 describes the relationship of SCLK and LCLK in various pixel modes.

Table 3-8. SCLK and LCLK Relationships

Multiplex Ratio	SCLK / LCLK Relationship
8:1	SCLK = LCLK = PCLK÷8
4:1	SCLK = LCLK = PCLK÷4
2:1	SCLK = LCLK = PCLK÷2
1:1	SCLK = LCLK = PCLK

GSD[31:0] is the input pixel data, 8 bits per pixel (4:1 MUX) and 4 bits per pixel (8:1 MUX) for four and eight horizontally consecutive output pixels. GSD[31:0] is always latched on the rising edge of LCLK.

The pixel clock is specified to be either PCLK0 or PCLK1 by bit 4 of the CSC register.

3.3.3.2 GSD[31:0] Mapping to Pixel Port Interface

Regardless of mode, the least significant word, byte, or nibble is the first to be displayed in time. For example, When in 4:1 mode, there are four 8 bit pixel ports, encoded within GSD[31:0]. Port GSD[7:0] corresponds to the first pixel of the first line of the display. This is the first pixel fed to the analog outputs, followed by GSD[15:8], then GSD[23:16], and finally GSD[31:24], repeating the pattern from LSB to MSB until the first scan line is completely displayed.

3.3.3.3 Odd/Even Field Definition

The output data sequence depends on bit 3, DM of the CSC register and the ODD/EVEN* input. For graphics data processing, the CL-PX2080 treats interlaced graphics data in the same manner as non interlaced data, merely transferring it for output processing. Interlaced data alignment is performed and controlled outside the CL-PX2080. Cursor Pattern Ram Data, however, is managed by the CL-PX2080 in interlaced mode.

In interlaced mode, scan line 1 is always displayed first and is considered the first line of the EVEN field. In non-interlaced mode, scan line 2 immediately follows scan line 1. In interlaced mode, scan line 2 is considered to be the first line of the ODD field and is displayed only after the entire EVEN field has been displayed and the ODD/EVEN* pin has toggled.

Only the ODD lines or only the EVEN lines will be displayed, if ODD/EVEN* does not change. Figure 3-10 shows the interlaced and non-interlaced display scan. Non-interlaced display scan is equal to one frame. Interlaced display scan is equal to one frame with odd and even fields.

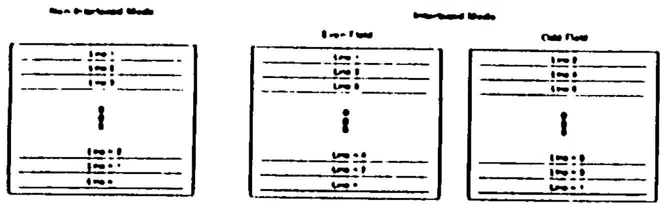

Figure 3-10. Interlaced and Non-Interlaced Display Scans

3.3.3.4 Pixel Read Mask Register

Each pixel clock cycle, GSD[31:0] pixel data is ANDed with the contents of the pixel read mask register and the result used to address the color palette RAM. The addressed location provides 24 bits of color information to the three D/A converters. Pixel masking is enabled for all modes of operation except when the true color by pass is enabled. The pixel mask register is not initialized during reset, and should be initialized by the user to 0FFh or another specific mask pattern for proper operation.

3.3.4 VRAM Port Modes of Operation

The 32-bit VRAM port can be used as a varying number of parallel pixel ports depending on the number of bits defined for each pixel. Following paragraphs describe the four possible combinations. In all cases, pixel data is latched on the rising edge of LCLK, and the least significant pixel is output first.

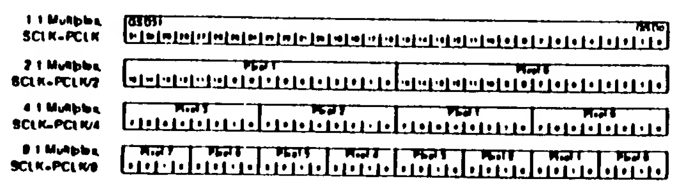

Figure 3-11. Pixel Mapping with Graphics Port

CL 42005

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Table 3-7. Pixel Index Mapping — Pixel Mask vs. VGA[7:0] and GSD[31:0] Bit Locations

Register/Format Type Description	MSB							LSB	Function
Pixel Mask Register	7	6	5	4	3	2	1	0	Register Bits
VGA Data	7	6	5	4	3	2	1	0	Palette Index
4 bits/pixel	x	x	x	x	3	2	1	0	Palette Index
8 bits/pixel	7	6	5	4	3	2	1	0	Palette Index
16 bits/pixel	14	13	12	11	10	x	x	x	Red Palette Index
5:5:5 Format	9	8	7	6	5	x	x	x	Green Palette Index
Sparse	4	3	2	1	0	x	x	x	Blue Palette Index
16 bits/pixel	x	x	x	14	13	12	11	10	Red Palette Index
5:5:5 Format	x	x	x	9	8	7	6	5	Green Palette Index
Contiguous	x	x	x	4	3	2	1	0	Blue Palette Index
16 bits/pixel	15	14	13	12	11	x	x	x	Red Palette Index
5:6:5 Format	10	9	8	7	6	5	x	x	Green Palette Index
Sparse	4	3	2	1	0	x	x	x	Blue Palette Index
16 bits/pixel	x	x	x	15	14	13	12	11	Red Palette Index
5:6:5 Format	x	x	10	9	8	7	6	5	Green Palette Index
Contiguous	x	x	x	4	3	2	1	0	Blue Palette Index
24 bits/pixel	23	22	21	20	19	18	17	16	Red Palette Index
8:8:8 Format	15	14	13	12	11	10	9	8	Green Palette Index
	7	6	5	4	3	2	1	0	Blue Palette Index

NOTE: LSB mapping is shown only to GSD[31:0]; pattern repeats to MSB.

3.3.4.1 16-Bits/Pixel Operation (1:1 MUX)

The 1:1 multiplexing mode is selected through bit 2, MR of the GFC register. In this mode, two independent 16-bit pixel ports, GSD[31:16] and GSD[15:0], are latched on the rising edge of LCLK, and are multiplexed 1:1. Bit 0, PS of the GFC register, selects between the two ports. One LCLK rising edge occurs every PCLK cycle. SCLK is equal to the current PCLK selected.

GSD[31] is used to switch between the two ports on a pixel-by-pixel basis when 5:5:5 RGB color format (bit 3, CF of the GFC register) and real-time pixel port switching is enabled (bit 1, TE of the GFC register). If PORTSEL is a logical zero, the VGA port is multiplexed regardless of the state of GSD[31]. GSD[15] is ignored internally when in 5:5:5 mode. Real-time pixel port switching is not supported for 5:6:5 RGB color format.

3.3.4.2 True Color Operation

Bit 4, TC, in the GFC register enables or disables the true color palette by pass feature. When by pass mode is selected, the pixel data are transferred directly to the proper MSBs of the respective DACs, by passing the palette and the pixel mask. When the by pass mode is not selected, the pixel data index the proper locations in the palette, and the correct color information is passed to the respective DACs. Bit 1, PM of the GSC register, selects sparse or contiguous palette mapping.

For sparse palette mapping, each independent color component of pixel data is mapped to the most significant bits of the respective palette entries; the least significant bits are set to zero. For contiguous palette mapping, each independent color component of the pixel data is mapped to the least significant bits of the respective palette address; the most significant bits are set to zero. For either sparse or contiguous mapping, the specified color palette values are transferred to the DACs.

When 5:5:5 or 5:6:5 color format is selected, the display may contain 32 K or 64K simultaneous colors respectively. The DACs can be configured for 6 or 8 bits of resolution in this mode.

Table 3.8. Color Mapping to QSD[31:0] Bus

Format	MSB G	R4	R3	R2	R1	R0	G4	G3	G2	G1	G0	B4	B3	B2	B1	LSB B0
5:5:5 Mode																
Port 1	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Port 2	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Format	MSB R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B4	B3	B2	B1	LSB B0
5:6:5 Mode																
Port 1	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Port 2	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

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Table 3.9. Operating Mode

	Pin QPS*	GFC Bit1 TE	GFC Bit0 PS	Pin QSD [31]	GFC Bit2 MR	GFC Bit3 CF	GFC Bit6 QPF1	GFC Bit5 QP10	Ports/Mux Order	Mux Rate
VGA	0	x	x	x	x	x	0	0	VGA[7:0]	1:1
4 bits/pixel	x	x	x	Data	x	x	1	1	QSD[3:0] QSD[7:4] QSD[11:8] QSD[15:12] QSD[19:16] QSD[23:20] QSD[27:24] QSD[31:28]	8:1
8 bits/pixel	x	x	x	Data	x	x	1	0	QSD[7:0] QSD[15:8] QSD[23:16] QSD[31:24]	4:1
16 bits/pixel(5:5:5) See Table Below	x	x	x	x	0	0	0	1	QSD[15:0] QSD[31:16]	2:1
16 bits/pixel(5:6:5) See Table Below	x	x	x	Data	0	1	0	1	QSD[15:0] QSD[31:16]	2:1
16 bits/pixel(5:5:5)	1	0	0	x	1	0	0	1	QSD[15:0]	1:1
16 bits/pixel(5:5:5)	1	0	1	x	1	0	0	1	QSD[31:16]	1:1
16 bits/pixel(5:6:5)	1	1	x	0	1	0	0	1	QSD[15:0]	1:1

3.3.5 Hardware Cursor Operation

The CL-PX2080 has an on-chip, three-color, user-definable cursor which is implemented in 32x32x2 bit memory. This cursor works in both interlaced and non-interlaced systems. The cursor can be programmed via the GFC register for three modes of operation which are summarized in Table 3.10 on page 46:

Table 3-10. Cursor 2-bit Data Decode vs. Mode Selected

Bit 1	Bit 0	Mode 1	Mode 2	Mode 3
0	0	Data	CC1	Data
0	1	CC1	CC2	Data
1	0	CC2	Color, Gamma Data	CC1
1	1	CC3	Inverse Data	CC2

CCn = Cursor Color Register n

The pattern for the cursor is provided by the cursor RAM, which may be accessed by the BIU at any time. Cursor positioning is performed in the Cursor position registers (CXH, CXL, CYH, CYL). Figure 3.12 demonstrates its usage.

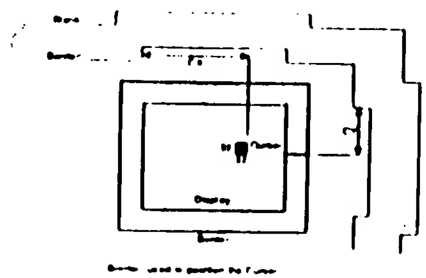

Figure 3.12 Cursor Operation

A value of (0,0) written to the cursor position registers places the cursor completely off screen, outside the viewing area. A cursor position value of (1,1) places the lower right pixel of the cursor on the upper left hand corner of the screen. Only one cursor pattern per frame is displayed, regardless of updates to the cursor position registers. The single restriction on position register updates is that all position registers must be written when the cursor location is updated.

The internal position register is updated when the Y upper byte(CYH) is written to ensure this operation. The cursor pattern is displayed at the last cursor location written prior to frame start. The reference point of the cursor, row 0 column 0, is the lower right corner of the cursor relative to BORDER*.

The position of the cursor is not dependent upon CBLANK*. The cursor X position is relative to the first rising edge of LCLK when BORDER* is sampled at a logical one. The cursor Y position is relative to the first rising edge of LCLK when BORDER* is sampled at logical one after vertical blanking period has been determined.

The cursor pattern can be displayed in a interlaced system if bit 3, DM of the CSC register, is a logical one. The first cursor line displayed (ROW 31 of cursor pattern RAM) depends on the state of the O/E* pin and the position value in CYH, CYL. If the Y position is an even number, the data in row 31 is displayed during the even field, starting at position (CX-31, CY-31), where CX is the concatenated position determined by CXH, CXL (and similarly with Y). Each subsequent scan line displayed in the even field corresponds to every alternate active cursor line after row 31 in the cursor RAM array. During odd fields, the even rows from the cursor pattern RAM are displayed starting with row 30 at position CX-31, CY-30). Each subsequent scan line displayed in the odd field corresponds to every alternate active cursor line after row 30 in the cursor RAM array.

Similarly, if the Y position value was an odd number in the first line displayed, then Row 31 and subsequent odd rows would be displayed during an odd field. Row 30 data and subsequent even rows would be displayed during the even field.

3.3.6 Internal Memory Access

Table 3-11. Memory Access Addressing and Indexing

Memory Access	Access Address BIR/PC Addr	Type R/W	Addressed by Register — BIR/PC Addr	Address Range	Mod 3 Counter bit 1,0
Color Palette RAM (red)	BIR-X, 0x03C9	W	LAW, BIR-X, 0x03C8	0x00 0xFF	00
Color Palette RAM (green)	BIR-X, 0x03C9	W	LAW, BIR-X, 0x03C8	0x00 0xFF	01
Color Palette RAM (blue)	BIR-X, 0x03C9	W	LAW, BIR-X, 0x03C8	0x00 0xFF	10
Color Palette RAM (red)	BIR-X, 0x03C9	R	LAR, BIR-X, 0x03C7	0x00 0xFF	00
Color Palette RAM (green)	BIR-X, 0x03C9	R	LAR, BIR-X, 0x03C7	0x00 0xFF	01
Color Palette RAM (blue)	BIR-X, 0x03C9	R	LAR, BIR-X, 0x03C7	0x00 0xFF	10
Gamma Palette RAM (red)	BIR-5, 0x27CD	W	VGW, BIR-5, 0x27CC	0x00 0xFF	00
Gamma Palette RAM (green)	BIR-5, 0x27CD	W	VGW, BIR-5, 0x27CC	0x00 0xFF	01
Gamma Palette RAM (blue)	BIR-5, 0x27CD	W	VGW, BIR-5, 0x27CC	0x00 0xFF	10
Gamma Palette RAM (red)	BIR-5, 0x27CD	R	VGR, BIR-5, 0x27CB	0x00 0xFF	00
Gamma Palette RAM (green)	BIR-5, 0x27CD	R	VGR, BIR-5, 0x27CB	0x00 0xFF	01
Gamma Palette RAM (blue)	BIR-5, 0x27CD	R	VGR, BIR-5, 0x27CB	0x00 0xFF	10
Cursor Pattern Ram - Bit 1	BIR-2, 0x27CB	W	LAW, BIR-X, 0x03C8	0x80 0xFF	N/A
Cursor Pattern Ram - Bit 0	BIR-2, 0x27CB	W	LAW, BIR-X, 0x03C8	0x00 0x7F	N/A
Cursor Pattern Ram - Bit 1	BIR-2, 0x27CB	R	LAR, BIR-X, 0x03C7	0x80 0xFF	N/A
Cursor Pattern Ram - Bit 0	BIR-2, 0x27CB	R	LAR, BIR-X, 0x03C7	0x00 0x7F	N/A
Border Color	BIR-1, 0x27CD	W	CAW, BIR-2, 0x27CC	xxxx xx00	00 10
Cursor Color 1	BIR-1, 0x27CD	W	CAW, BIR-2, 0x27CC	xxxx xx01	00 10
Cursor Color 2	BIR-1, 0x27CD	W	CAW, BIR-2, 0x27CC	xxxx xx10	00 10
Cursor Color 3	BIR-1, 0x27CD	W	CAW, BIR-2, 0x27CC	xxxx xx11	00 10
Border Color	BIR-1, 0x27CD	R	CAR, BIR-2, 0x27CB	xxxx xx00	00 10
Cursor Color 1	BIR-1, 0x27CD	R	CAR, BIR-2, 0x27CB	xxxx xx01	00 10
Cursor Color 2	BIR-1, 0x27CD	R	CAR, BIR-2, 0x27CB	xxxx xx10	00 10
Cursor Color 3	BIR-1, 0x27CD	R	CAR, BIR-2, 0x27CB	xxxx xx11	00 10

3.3.6.1 Color RAM Data Access

Color palette, gamma palette, cursor and cursor border colors are specified in terms of 24-bit RGB data, one byte per color. The host processor accesses a color memory location by first writing the index address, then performing three successive writes or reads to the data register. Upon completion of the third access, the index register points to the next location.

For example, to update the color palette data, the processor writes the CL-PX2080 address register (RAM write mode) with the address of the color palette RAM location to be modified. The processor performs three successive write cycles (8 bits each of red, green, and blue). After the blue write cycle, the three bytes of color information are concatenated into a 24-bit word and written to the location specified by the address register. The address register then increments to the next location, which the processor can modify by simply writing another sequence of red, green, and blue data. To write to a block of color values in consecutive locations, write the start address and perform continuous R, G, B write cycles until the entire block has been written. Cursor and other color information is handled the same way. Refer to appropriate Bus Interface Unit configuration for read/write timing.

3.3.8.2 VGA Compatible Access Modes

The CL-PX2080 has the flexibility to operate in a system with a separate VGA controller/DAC or to operate as the sole display output. Many currently used VGA/DAC ICs internally decode the ISA standard addresses for the palette RAM. The CL-PX2080 is capable of transparently replacing an existing DAC, operating in parallel, or operating as a separate subsystem at a unique address. Three access modes are available to maintain compatibility with software designed for VGA registers.

Mode 0 is for a system with a separate pre-existing VGA controller and palette DAC. Graphic data from the auxiliary or "feature" connector of the existing controller board enters the VGA graphics port of the CL-PX2080, where it is mixed with video data from an external source. As shown in Figure 3-13, a single

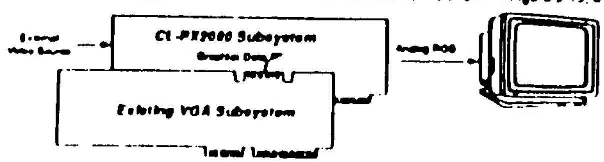

Figure 3-13. Mode 0 System Configuration

external monitor is connected to the analog RGB output of the CL-PX2080. In order to preserve the same functionality with all VGA software drivers, the CL-PX2080 must accept writes to the standard VGA palette addresses, but not respond to reads, allowing the existing VGA controller board to respond. The CL-PX2080 palette RAM shadows the VGA controller RAM on writes only. Mode 0 is also useful in designs configured like that shown in Figure 3-14, when the CL-PX2080 is used with a self decoding VGA controller.

Mode 1 is designed for a system which has a VGA controller/palette DAC and a CL-PX2080 in the same subsystem. Graphic data from the auxiliary, or "feature" connector of the existing controller board enters the VGA graphics port of the CL-PX2080, where it is mixed with video data from an external source, as

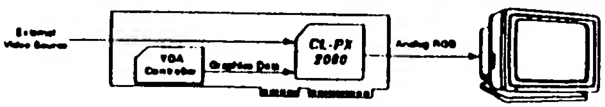

Figure 3-14. Mode 1 System Configuration

shown in Figure 3-13. The difference between modes 0 and 1 is that mode 1 responds to reads at the

CL 42008

May 1991

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palette RAM address. This system is compatible with existing software that manipulates the VGA palette RAM.

Mode2 is designed for a system containing a VGA controller (with palette DAC) and a CL-PX2080 subsystem, each driving separate RGB monitors, as shown in Figure 3-15. In this scenario the VGA subsystem

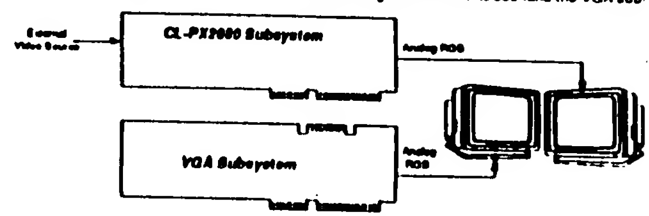

Figure 3-15. Mode 2 System Configuration

system occupies the standard VGA palette RAM addresses and the CL-PX2080 registers respond to a completely separate set of addresses.

Modes are selected by the EI, RE and RO bits in the BIR register, described in Section 4.1.1 on page 87.

3.3.8.3 Additional Information

When accessing the color palette RAM, the address register resets to 00h following a blue read or write to RAM location FFh.

The processor interface operates asynchronously to the pixel clock. Data transfers between the color palette RAM and the color registers (R,G, and B in the block diagram) are synchronized by internal logic, and occur in the period between processor accesses. To reduce noticeable sparking on the CRT screen during processor access to the color palette RAMS, internal logic maintains the previous output color data on the analog outputs while the transfer between RGB registers and Look-Up Table RAMs occurs.

To keep track of the red, green, and blue read/write cycles, the address register has two additional bits (bit1, bit0) that count modulo three. They are reset to zero when the processor writes to the address register, and are not reset to zero when the processor reads the address register. The processor does not have access to these bits. The processor can read the address register at any time without modifying its contents or the existing read/write mode.

3.3.8.4 Accessing the Cursor RAM Array

The 32x32x2 cursor RAM is accessed in a planar format where plane 1 is bit1 of the cursor data and plane 0 is bit0. In the planar format, only 7 address bits are used. The eighth bit is to determine which plane (0

or 1) data of the cursor RAM array is accessed (see Figure 3-11). A single address presented in the cursor RAM accesses 8 bit locations in plane 0 or 1, depending on the state of address bit 7.

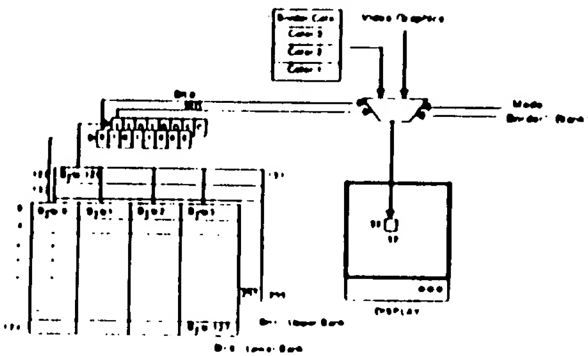

Figure 3-10. Cursor RAM Function Diagram

After each access in the planar format, the address increments. The processor uses LAW or LAR (write or read) binary address counters to access the cursor RAM array (see Table 2). Note that LAW (LAR) is the same binary counter used for RGB auto incrementing access to the color palette RAM. Any write to LAW after cursor auto incrementing has been initiated resets the cursor auto incrementing logic until cursor RAM array has been accessed again. Cursor auto incrementing then begins from the address written. A read from the LAR does not reset the cursor auto-incrementing logic. The color palette RAM and the cursor RAM share the same internal address registers, and processor addressing for this and all other registers is determined by the appropriate register addresses documented in Section 4, Registers.

Table 3-12. Cursor Memory Mapping and Relationships for Display

Bit 1	Bit 0	Mode 1	Mode 2	Mode 3
0	0	Data	CC1	Data
0	1	CC1	CC2	Data
1	0	CC2	Data	CC1
1	1	CC3	Not Data	CC2

NOTE CCn = Cursor Color Register n
Data = Color or Gamma Palette Data
Not = Inverse of

CL 42009

May 1991

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3.3.6.5 6-Bit / 8-Bit Operation

Bit 1, D24/16 of the ABC register, is used to specify whether the processor is reading and writing 8 bits or 6 bits of color information each cycle.

For 8 bit operation, D0 is the LSB and D7 is the MSB of color data.

For 6 bit operation, color data is contained on the lower 6 bits of the data bus, with D0 being the LSB and D5 the MSB of the color data. When writing color data, D6 and D7 are ignored. During color read cycles, D6 and D7 are logical zero. Accessing the cursor RAM array does not depend on the resolution of the DACs.

Note that in the 6 bit mode, the CL-PX2080's full-scale output current will be less than when it is in the 8 bit mode, since the two LSBs of each 8 bit DAC are always a logical zero in the 6 bit mode.

3.3.7 Mixing to Output DAC

The Output DAC contains three 85 MHz 8 bit digital to analog converters. The table below shows how the graphic data path is controlled at the input of the DAC by BORDER*, BLANK*, and GPS.

Table 3-13.

BLANK*	BORDER*	GPS	
0	X	X	Video blanking
1	0	X	Border color
1	1	0	VGA or cursor color
1	1	1	OSD or cursor color

The GPS pin is an input used to select between the VGA and Serial graphics ports for graphics data input. BLANK* and BORDER* both prevent Graphics and Video data from being presented to the DAC. If the GPS pin is not used, it should be tied to the appropriate logical value for the graphics port selected.

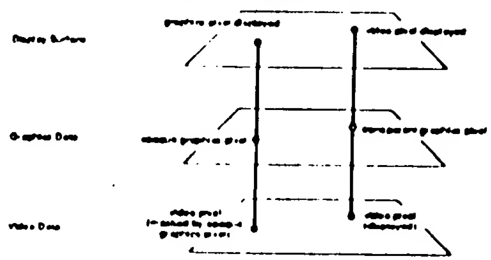
3.3.7.1 Graphics Overlay Control

The graphics overlay controls consist of a 32-bit color key, a 32-bit color key mask, an 8-bit overlay op code, and an 8:1 multiplexer.

To understand how the graphics overlay controls work, imagine the CL-PX2080 as managing two images, one in front of the other. The two image planes are the video and graphics images, with the video image behind the graphics image. Every graphics pixel is either transparent or opaque. If the graphics pixel is opaque, the graphics color information for that pixel is displayed on the screen. If the graphics pixel is transparent, the color information of the video pixel behind it is displayed on the screen.

The graphics overlay controls determine which graphics pixels are transparent. The determination is made by a combination of two overlay control features: a TAG bit component in the video pixel data, and the graphics COLOR key switch. The graphics COLOR key switch is generated by ANDing the graphics pixel data with the GKM register, and then comparing the results against the GCK register. The tag bit is

generator to create the CL-PX2080. The resulting switches are the select lines to the multiplexer, while the Graphics Overlay OpCode (GOC) register is the input to the multiplexer.



3.3.7.2 Graphics Overlay OpCode Register (GOC)

The Graphics Overlay OpCode is an 8-bit value used as input to an 8:1 multiplexer. The select signals to the multiplexer (the TAG bit and the graphics COLOR key match) determine which of the eight bits will become the transparency control for each pixel time. If a bit in the GOC register is , the graphics pixel becomes transparent, enabling the video pixel for final display. The GOC register is initialized to 0x00 during reset, selecting the graphics path and ignoring the video input stream.

3.3.8 CLK Synchronizer and SYNC Alignment

The Clock generator creates all device clocks. The rising edge of LCLK latches OSD[31:0] or VOA[7:0], and BLANK*, HSIN, VSIN, GPS and BORDER*. The information latched by this signal is synchronized internally with SCLK. To avoid metastability, LCLK must maintain setup and hold requirements to SCLK. Data is synchronized with the selected pixel clock (PCLK0 or PCLK1) after being internally latched with SCLK. When the input data multiplexing rate is 8:1, 4:1, 2:1, or 1:1, LCLK must be the pixel clock divided by 8, 4, 2 or 1 respectively.

The SYNC alignment circuitry generates external HSOUT and VSOUT signals required for the monitor. The output is delayed to match the internal PCLKn delay of the RGB outputs. A SYNC Alignment Register is provided to program polarities of HSIN, HSOUT, VSIN, VSOUT. This register also generates a programmable PCLKn delay of RGB relative to the matched HSOUT and VSOUT, described above. This delay is programmable in both directions.

3.3.9 Power-Down Mode

The CL-PX2080 incorporates a power-down mode, controlled by bit 6 and 0 of the ASC register. While bit 6 (CKOFF) and bit 0 (DAOFF) are logical zeroes, the CL-PX2080 functions normally.

While bit 6 (CKOFF) is a logical one, all clock inputs, PCLKn, VCLK and LCLK, are disabled.

While bit 0 (DAOFF) is a logical one, the DACs and power to the RAM are turned off.

Note that the RAM still retains the data. Also, the RAM can be read or written to by the processor as long as the pixel clock is running. The RAM automatically powers up during processor read/write cycles, and shuts down when the processor access is completed. The DACs output no current, and the three command registers can still be written to or read by the processor.

Note that the output DACs require about one second to turn off (sleep mode) or turn on (normal), depending on the compensation capacitor used.

The DACs will be turned off during sleep mode only if a voltage reference (internal or external) is used.

External circuitry should turn off the current reference (IREF = 0) to further reduce power consumption due to biasing of portions of the internal current reference.

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CL 42011

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4. REGISTERS

Internal registers control the operations of the CL-PX2080. These registers are organized in mapping order in Table 4-1 on page 57. Table 5-2 on page 72 summarizes the CL-PX2080 registers, and organizes them according to the following functions:

- Indexing
- CLUT Access
- Cursor Access
- Video, Graphics, and Cursor Control
- Video Gamma Correction Palette Access
- Graphics Overlay Control
- Cursor Positioning
- Digital to Analog Conversion and Controls

NOTE Data values reserved register locations are not guaranteed on readback. Reserved bits in used register locations are read back as 0.

Table 4-1. CL-PX2080 Control Registers (Organized by Mapping)

NOTE RS[4:0] is direct addressing in coprocessor mode. I/O address and BIR (Base Index Register) apply to ISA and MCA modes.

Register	RS[4:0]	Pri. I/O Addr	Sec Addr	BIR	Definition	Ref. Section
BIR	N/A	0x27CE	0x029E	N/A	Block Index Register	4.1.1, p. 58
LAW	0x00	0x03C8	N/A	N/A	CLUT Write Address	4.2.1, p. 60
LCD	0x01	0x03C9	N/A	N/A	CLUT Color Data	4.2.2, p. 61
LPM	0x02	0x03C6	N/A	N/A	CLUT Pixel Mask	4.2.3, p. 62
LAR	0x03	0x03C7	N/A	N/A	CLUT Read Address	4.2.4, p. 63
CAW	0x04	0x27CC	0x029C	1	Cursor Address Write	4.3.1, p. 64
CCD	0x05	0x27CD	0x029D	1	Cursor Color Data Registers	4.3.2, p. 64
ASC	0x06	0x27CA	0x029A	1	Analog Setup Control	4.8.1, p. 79
CAR	0x07	0x27CB	0x029B	1	Cursor Address Read	4.3.3, p. 65
GFC	0x08	0x27CC	0x029C	2	Graphics Format Control	4.4.2, p. 67
CSC	0x09	0x27CD	0x029D	2	Cursor Setup Control	4.4.3, p. 68
GSR	0x0A	0x27CA	0x029A	2	Graphics Status Register	4.4.1, p. 66
CPR	0x0B	0x27CB	0x029B	2	Cursor Pattern RAM	4.3.4, p. 65
CXL	0x0C	0x27CC	0x029C	3	Cursor X Position, Low Byte	4.7.1, p. 75
CXH	0x0D	0x27CD	0x029D	3	Cursor X Position, High Byte	4.7.1, p. 75

Table 4-1. CL-PX2080 Control Registers (Organized by Mapping)

NOTE: RS[4:0] is direct addressing in coprocessor mode. I/O address and BIR (Base Index Register) apply to ISA and MCA modes.

Register	RS[4:0]	Pri IO Addr	Sec Addr	BIR	Definition	Ref Section
CYL	0x0E	0x27CB	0x029B	3	Cursor Y Position, Low Byte	4.7.2 p 70
CYH	0x0F	0x27CB	0x029B	3	Cursor Y Position, High Byte	4.7.2 p 70
VFC	0x10	0x27CC	0x029C	4	Video Format Control	4.7.3 p 77
GOC	0x11	0x27CD	0x029D	4	Graphics Overlay Opcode	4.8.1 p 72
SAR	0x12	0x27CA	0x029A	4	SYNC Alignment Register	4.7.4 p 78
RSV1	0x13	0x27CB	0x029B	4	Reserved Register 1	4.10.8 page 80
VGW	0x14	0x27CC	0x029C	5	Video Gamma Write	4.9.1 p 69
VGD	0x15	0x27CD	0x029D	5	Video Gamma Correction Data	4.9.2 p 70
RSV2	0x16	0x27CA	0x029A	5	Reserved Register 2	4.7 p 75
VGR	0x17	0x27CB	0x029B	5	Video Gamma Address Read	4.9.3 p 71
GCKR	0x18	0x27CC	0x029C	6	Graphics Chroma Key Red	4.8.2 p 73
GCKG	0x19	0x27CD	0x029D	6	Graphics Chroma Key Green	4.8.2 p 73
GCKB	0x1A	0x27CA	0x029A	6	Graphics Chroma Key Blue	4.8.2 p 73
RSV3	0x1B	0x27CB	0x029B	6	Reserved Register 3	4.10.2, page 89
GKMR	0x1C	0x27CC	0x029C	7	Graphics Key Mask Red	4.8.3 p 74
GKMG	0x1D	0x27CD	0x029D	7	Graphics Key Mask Green	4.8.3 p 74
GKMB	0x1E	0x27CA	0x029A	7	Graphics Key Mask Blue	4.8.3, p 74
RSV4	0x1F	0x27CB	0x029B	7	Reserved Register 4	4.10.4, page 83

4.1 Indexing

4.1.1 BIR: Block Index Register

IO Address	(ISA, MCA Modes)	0x02E0
Base Index Register	(ISA, MCA Modes)	N/A
Direct Address	(Coprocessor Mode)	N/A

Block Index Register BIR specifies one of eight 4-register banks which can be directly read and written at 16-bit PC port addresses 0x27CA-0x27CD. The CLUT access registers LAW, LCD, LPM, and LAR are

CL 42013

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the exception. BIR is used only in ISA and MCA bus modes; it is not accessible in coprocessor bus mode, when all registers are addressed directly through RS[4:0].

IE	RE	SE	RO	RSVD	BLK2	BLK1	BLK0
7	6	5	4	3	2	1	0

Bit #	Access	Reset		Description
7	R/W	0	IE	Index Enable 1 Indexed addressing 0 Direct addressing
6	R/W	0	RE	Read Only Enable 1 VGA read only access 0 VGA read/write access
5	R/W	0	SE	Secondary address enable 1 Secondary address range 0 Primary address range
4	R/W	0	RO	03C7h Read Override 1 Read enabled at 03C7h 0 Read disabled at 03C7h
3	R/W	0	RSVD	Reserved
2	R/W	0	BLK2	Block Select 2
1	R/W	0	BLK1	Block Select 1
0	R/W	1	BLK0	Block Select 0

Table 5-1. Read access for VGA Compatibility Modes

IE (7)	RE (6)	RO (4)	03C7h read access	03C6h, 03C8h, 03C9h read access
0	0	x	disabled	disabled
0	1	0	disabled	enabled
0	1	1	enabled	enabled
1	x	x	enabled at Indexed address via BLK[2:0]	

4.2 CLUT Access

The graphics Color Look Up Table (CLUT) expands 4-, 8-, and 16-bit graphics pixel data to 18 or 24 bits of color data. Access modes are described in 3.3.8.2, p. 30.

4.2.1 LAW: CLUT Write Address

I/O Address	(ISA, MCA Modes)	0x03C8
Base Index Register	(ISA, MCA Modes)	N/A
Direct Address	(Coprocessor Mode)	0x00

CLUT Write Address Register LAW, a modulo 256 counter, shares two functions — palette color selection and cursor pattern selection.

Palette Color Selection

In palette color selection mode, LAW specifies the 24- or 18-bit graphics palette color to be written to register LCD on the next write operation. LAW specifies the same palette color for write cycles R, G, and B. After write cycle B, LAW automatically increments by one to specify the next palette color.

WA							
7	6	5	4	3	2	1	0

Bit #	Access	Reset		Description
7:0	R/W	0h	WA	Write Access for palette RAM

Cursor Pattern Selection

In cursor pattern selection mode, LAW addresses the cursor pattern RAM, which comprises two 32x32 bit or 4x32 byte planes, for a total of 128 bytes in each plane. LAW automatically increments when writing to register CPR.

P	WA						
7	6	5	4	3	2	1	0

Bit #	Access	Reset		Description
7	R/W	0	P	Plane. Specifies the cursor bit plane to be addressed 0 LSB plane of cursor ram 1 MSB plane of cursor ram
6:0	R/W	0h	WA	Write Address for cursor RAM. Byte address of cursor pixels (8 per address) being addressed for the 128 bytes in cursor RAM. Bytes 3:0 are the four bytes of the top row.

CL 42014

80

May 1991

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4.2.2 LCD: CLUT Color Data

I/O Address	(ISA, MCA Modes)	0x03C9
Base Index Register	(ISA, MCA Modes)	N/A
Direct Address	(Coprocessor Mode)	0x01

Port LCD is an 8-bit wide path to the graphics color palette — a 256x18- or 24-bit memory array. LCD must be addressed three times, once for each palette color.

For read operations:

- The first read operation reads the red 6- or 8-bit component (as specified by register ASC, bit D24) of the palette color specified by LAR.
- The second read operation reads the green 6- or 8-bit component of the palette color specified by LAR.
- The third read operation reads the blue 6- or 8-bit component of the palette color specified by LAR.

After the blue component is read, register LAR automatically increments to the next palette color. When in 6-bit mode, the data shifts left two bits, and the two LSBs are padded with zeros before loading into the palette.

For write operations:

- The first write operation writes the red 6- or 8-bit component of the palette color specified by LAW.
- The second write operation writes the green 6- or 8-bit component of the palette color specified by LAW.
- The third write operation writes the blue 6- or 8-bit component of the palette color specified by LAW.

After the blue component is written, register LAW automatically increments to the next palette color. When in 6-bit mode, the data shifts left two bits and the two LSBs are padded with zeros before loading into the palette.

D							
7	6	5	4	3	2	1	0

Bit #	Access	Reset		Description
7:0	R/W	0h	D	Color LUT Data.

4.2.3 LPM: CLUT Pixel Mask

I/O Address	(ISA, MCA Modes)	0x03C6
Base Index Register	(ISA, MCA Modes)	N/A
Direct Address	(Coprocessor Mode)	0x02

The graphics pixel data used to look up color information in the palette can be masked before the lookup takes place. Register LPM masks the address. The 6- or 8-bit graphics pixel is logically ANDed with the LPM data, and the result is used to address the color palette.

M							
7	6	5	4	3	2	1	0

Bit #	Access	Reset		Description
7:0	R/W	ffh	M	CLUT Pixel Mask.

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CL 42015

4.2.4 LAR: CLUT Read Address

I/O Address	(ISA, MCA Modes)	0x03C7
Base Index Register	(ISA, MCA Modes)	N/A
Direct Address	(Coprocessor Mode)	0x03

CLUT Read Address register LAR is a modulo 256 counter that shares two functions: palette color selection and cursor pattern selection.

Palette Color Selection

In palette color selection mode, LAR specifies the 24- or 18-bit graphics palette color to be read on the next read operation to register LCD. LAR specifies the same palette color for read cycles R, G, and B. After read cycle B, LAR automatically increments by one to specify the next palette color.

RA							
7	6	5	4	3	2	1	0

Bit #	Access	Reset		Description
7:0	R/W	0	RA	CLUT Read Address.

Cursor Pattern Selection

In cursor pattern selection mode, LAR addresses the cursor pattern RAM, which comprises two 32x32 bit or 4x32 byte planes, for a total of 128 bytes in each plane. LAR automatically increments when writing to register CPR.

P	RA						
7	6	5	4	3	2	1	0

Bit #	Access	Reset		Description
7	R/W	0	P	Plane. Specifies the cursor bit plane to be addressed. 0 LSB plane of cursor RAM 1 MSB plane of cursor RAM
6:0	R/W	0	RA	CLUT Read Address. Byte address of cursor pixels (8 per address) being addressed for the 128 bytes in cursor RAM. Bytes 3:0 are the four bytes of the top row. 0 The LSB plane of cursor RAM. 1 The MSB plane of cursor RAM.

4.3 Cursor Access

4.3.1 CAW Cursor Address Write

I/O Address	(ISA, MCA Modes)	0x02EC
Base Index Register	(ISA, MCA Modes)	1
Direct Address	(Coprocessor Mode)	0x04

Cursor Address Write register (CAW) is a modulo 4 counter that specifies the 24 bit cursor or border color register that is to be modified on the next write operation to register CCD. CAW specifies the same cursor color register for write cycles R, G, and B. After write cycle B, CAW automatically increments by one to specify the next cursor color register.

RSVD						WA	
7	6	5	4	3	2	1	0

Bit #	Access	Reset		Description
7:2	R/W	0h	RSVD	Reserved (write as zero)
1:0	R/W	0	WA	Cursor Write Address

4.3.2 CCD Cursor Color Data Registers

I/O Address	(ISA, MCA Modes)	0x02ED
Base Index Register	(ISA, MCA Modes)	1
Direct Address	(Coprocessor Mode)	0x05

See also Table 3.11, Memory Access Addressing and Indexing, p. 48
Figure 3.13 Cursor RAM Function Diagram, p. 49

Port CCD accesses three 24 bit cursor and border color registers.

- For cursor color read operations, register CAR must point to the cursor color to be read.
- For cursor color write operations, register CAW must point to the cursor color to be written.

CAR and CAW point to the red component of each color only.

Three I/O operations — R, G, and B — must take place for each color. CAR and CAW automatically increment by one after I/O operation B. The components must be read and/or written in the following order: red, green, blue.

D							
7	6	5	4	3	2	1	0

Bit #	Access	Reset		Description
7	R/W	0	D	Color Data.

CL 42016

4.3.3 CAR Cursor Address Read

I/O Address	(ISA, MCA Modes)	0x02EB
Base Index Register	(ISA, MCA Modes)	1
Direct Address	(Coprocessor Mode)	0x07

Register CAR is a modulo-4 counter that specifies the 24-bit cursor color register to be read on the next read operation to register CCD. CAR specifies the same cursor color register for read cycles R, G, and B. After read cycle B, CAR automatically increments by one to specify the next cursor color register.

RSVD						RA	
7	6	5	4	3	2	1	0

Bit #	Access	Reset		Description
7:2	R/W	0h	RSVD	Reserved (write as zero)
1:0	R/W	0	RA	Cursor Read Address.

4.3.4 CPR: Cursor Pattern RAM

I/O Address	(ISA, MCA Modes)	0x02EB
Base Index Register	(ISA, MCA Modes)	2
Direct Address	(Coprocessor Mode)	0x08

Registers LAW and LAR address register CPR. The cursor pattern RAM comprises two 32x32 bit (or 4x32 byte) planes, for a total of 128 bytes for each plane. A write or read to the CPR writes or reads the cursor pattern data.

D							
7	6	5	4	3	2	1	0

Bit #	Access	Reset		Description
7:0	R/W	0	D	Cursor Pattern RAM Data.

4.4 Video, Graphics, and Cursor Control

4.4.1 GSR Graphics Status Register

I/O Address	(ISA, MCA Modes)	0x021A
Base Index Register	(ISA, MCA Modes)	2
Direct Address	(Coprocessor Mode)	0x0A

Read only register GSR is a modulo 3 counter that sets up and monitors the CL-PX2080 revisions and I/O cycles.

REV				S	IO	CP	
7	6	5	4	3	2	1	0

Bit #	Access	Reset		Description
7-4	Read Only	0h	REV	Revision level. Current REV=0000
3	Read Only	0	S	Sense bit status 0 — All analog outputs are below the 335 mV level 1 — At least one of the analog outputs have exceeded the 335 mV level
2	Read Only	0	IO	I/O read/write access status 0 — LAW, CAW, or VDW has been specified (write mode) 1 — LAR, CAR, or VDR has been specified (read mode)
1-0	Read Only	00	CP	Color Pointer. Color component to be accessed by Host on next I/O cycle to a palette 00 — Red is specified 01 — Green is specified 10 — Blue is specified

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CL 42017

4.4.2 GFC Graphics Format Control

I/O Address	(ISA, MCA Modes)	0x02EC
Base Index Register	(ISA, MCA Modes)	2
Direct Address	(Coprocessor Mode)	0x08

Register GFC sets up the graphic interface timing and color format controls.

RD*	GPF		TC	CF	MR	TE	PS
7	6	5	4	3	2	1	0

Bit #	Access	Reset		Description
7	R/W	0	RD*	RD* pin disable 0 — Tristate AD bus on all register read operation 1 — Normal operation, all registers are readable
6-5	R/W	00	GPF	Graphics Port Format. Selects data type: 00 — 24 bit pixel 8:8:8 RGB data (PCLK:LCLK = 1:1) 01 — 16 bit pixel mode (mux ratios set by bit 2 of GFC) 10 — Four 8-bit pixels (PCLK:LCLK = 4:1) 11 — Eight 4-bit pixels (PCLK:LCLK = 8:1)
4	R/W	0	TC	True Color graphics palette by-pass: 0 — Pixel data is pseudocolor; PS, TE, MR, CF are ignored 1 — Pixel data is true color.
3	R/W	0	CF	Color Format. Controls 16-bit graphics port RGB color format 0 — 5:6:5 1 — 6:6:5
2	R/W	0	MR	Multiplexing Rate. Controls 16-bit graphics port data multiplexing rate 0 — The PCLK to LCLK ratio is 2:1 (two pixel bus) 1 — The PCLK to LCLK ratio is 1:1 (one pixel bus).
1	R/W	0	TE	Tag Enable. Specifies graphics 5:5:5 RGB 1:1 mux data mode pixel selector: 0 — Bit 0 in Register GFC is pixel selector. 1 — GSD[31:0] is video pixel selector in the 5:5:5 RGB graphics data mode.
0	R/W	0	PS	Pixel Selector. Selects Graphics pixel for 5:6:5 and 5:5:5 RGB 1:1 mux data: 0 — Graphics pixel 0 (graphics data on port GSD[15:0]). 1 — Graphics pixel 1 (graphics data on port GSD[31:16])

4.4.3 CSC: Cursor Setup Control

I/O Address	(ISA, MCA Modes)	0x021D
Base Index Register	(ISA, MCA Modes)	7
Direct Address	(Coprocessor Mode)	0x09

Register CSC sets cursor modes and controls palette indexing for 16 bit graphics data modes and clock selections.

SD	OPS		CS	DM	PM	CMS	
7	6	5	4	3	2	1	0

Bit #	Access	Reset		Description
7	R/W	0	SD	SCLK Disable 0 SCLK is enabled 1 SCLK is disabled
6-5	R/W	00	OPS	Graphics data Port Select on pin enable 00 Pin OPS is disabled (VGA port always selected) 01 Pin OPS is enabled (VGA or Serial Graphics port) 10 Pin OPS is disabled (Serial Graphics port selected always) 11 Pin OPS is disabled (Serial Graphics port to output VGA input)
4	R/W	0	CS	Pixel Clock Selection 0 PCLK0 is selected 1 PCLK1 is selected
3	R/W	0	DM	Display Mode 0 Progressive scan displays 1 Interlaced scan displays
2	R/W	0	PM	Palette Mapping for 16 bit graphics data to 18 bit DAC. 0 Color components are mapped to MSBs of their appropriate palettes 1 Color components are mapped to LSBs of their appropriate palettes All unused bits of color components are padded with zeros
1-0	R/W	00	CMS	Cursor Mode Select 00 Cursor disabled 01 Three color cursor 10 Two color cursor with highlighting 11 Two color cursor

4.5 Video Gamma Correction Palette Access

The video gamma correction palette is a 256x24-bit memory array that maps non-linear video pixel data to linear color data. The Gamma palette is accessed through registers VGR, VGD and VGW when register BIR = 5

4.5.1 VGW: Video Gamma Write

I/O Address	(ISA, MCA Modes)	0x02EC
Base Index Register	(ISA, MCA Modes)	5
Direct Address	(Coprocessor Mode)	0x14

Register VGW is a modulo-256 counter that specifies the 24-bit video gamma palette color to be written on the next write operation to register VGD. VGW points to the same palette color for write cycles R, G, and B. After the write cycle B, it automatically increments by one to specify the next palette color.

WA							
7	6	5	4	3	2	1	0

Bit #	Access	Reset		Description
7-0	R/W	0h	WA	Write Address. Byte address of gamma palette RAM

CL 42018

68

May 1991

4.9.2 VGD Video Gamma Correction Data

I/O Address	(ISA, MCA Modes)	0x02ED
Base Index Register	(ISA, MCA Modes)	8
Direct Address	(Coprocessor Mode)	0x19

The VGD port is an 8 bit wide path to the graphics color palette (a 256x24 bit memory array) and must be addressed three times for each palette color.

For read operations:

- The first read operation reads the red 8 bit component of the palette color specified by VGR.
- The second read operation reads the green 8 bit component of the palette color specified by VGR.
- The third read operation reads the blue 8 bit component of the palette color specified by VGR.

After the blue component is read, register VGR automatically increments to the next palette color. When in 8 bit mode, the data shifts left two bits and the two LSBs are padded with zeros before loading into the palette.

For write operations:

- The first write operation writes the red 8 bit component of the palette color specified by VGW.
- The second write operation writes the green 8 bit component of the palette color specified by VGW.
- The third write operation writes the blue 8 bit component of the palette color specified by VGW.

After the blue component is written, register VGW automatically increments to the next palette color.

D							
7	6	5	4	3	2	1	0

Bit #	Access	Reset		Description
7:0	R/W	0	D	Video gamma correction Data

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CL 42019

4.9.3 VGR Video Gamma Address Read

I/O Address	(ISA, MCA Modes)	0x02EB
Base Index Register	(ISA, MCA Modes)	8
Direct Address	(Coprocessor Mode)	0x17

Register VGR is a modulo-256 counter that specifies the next 24-bit video gamma palette color to be read on the next read operation to register VGD. VGR specifies the same palette color for read cycles R, G, and B. After the read cycle B, it automatically increments by one to specify the next palette color.

RA							
7	6	5	4	3	2	1	0

Bit #	Access	Reset		Description
7:0	R/W	0h	RA	Read Address. Byte address of gamma palette RAM

4.8 Graphics Overlay Control

The graphics overlay controls comprise:

- an 8 bit Graphics Overlay Opcode — register GOC;
- a 32 bit Graphics Chroma Key — registers GCKc;
- a 32 bit Graphics Key Mask — registers GKMc;
- an 8:1 multiplexer.

The CL-PX2080 can be viewed as a dual image formatter. The graphics image is in front, the video image is in back.

Every graphics pixel is either opaque or transparent.

- If the graphics pixel is opaque, its graphics color information is displayed on the screen.
- If the graphics pixel is transparent, the color information of the video pixel behind it is displayed on the screen.

The graphics overlay controls determine which graphics pixels are transparent, based on a combination of two overlay control features:

- a TAG bit component in the video pixel data, which is generated outside the CL-PX2080;
- the graphics COLOR key switch, which is generated by ANDing the graphics pixel data with the GKM register, then comparing the results against the GCK register.

4.8.1 GOC: Graphics Overlay Opcode

I/O Address	(ISA, MCA Modes)	0x021D
Base Index Register	(ISA, MCA Modes)	4
Direct Address	(Coprocessor Mode)	0x11

GOC is an 8 bit value that inputs to an 8:1 multiplexer. The select signals to the multiplexer — the TAG bit and the graphics COLOR key match — determine which of the eight bits become the transparency control for each pixel time. A high bit in register GOC enables video and makes graphics transparent. This value selects the graphics path and ignores video input stream.

T							
7	6	5	4	3	2	1	0

Bit #	Access	Reset		Description
7:0	R/W	nn	T	Transparency. Graphics pixel transparency control bit map for f(TAG, COLOR), as shown in Table 5.2 on page 72 1 Select video pixel for function 0 Select graphics pixel for function

Table 5.2 GOC Control Bit Mapping

TAG	COLOR	GOC Control Bit
0	0	10
0	1	11
1	0	12
1	1	13
0	0	14
0	1	15
1	0	16
1	1	17

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CL 42020

4.8.2 GCKc: Graphics Chroma Key

I/O Address	(ISA, MCA Modes)	0x02EC (GCKR: Graphics Chroma Key Red) 0x02ED (GCKG: Graphics Chroma Key Green) 0x02EA (GCKB: Graphics Chroma Key Blue)
Base Index Register	(ISA, MCA Modes)	8 (GCKR: Graphics Chroma Key Red) 8 (GCKG: Graphics Chroma Key Green) 8 (GCKB: Graphics Chroma Key Blue)
Direct Address	(Coprocessor Mode)	0x18 (GCKR: Graphics Chroma Key Red) 0x19 (GCKG: Graphics Chroma Key Green) 0x1A (GCKB: Graphics Chroma Key Blue)

Registers GCKR, GCKG, and GCKB control the Graphics Chroma Key function.

- When the CL-PX2080 uses the 8-bit VGA port for graphics data, the data in registers GCKc is compared against four adjacent graphics pixels. GCKR is compared to the least significant pixel.
- When the CL-PX2080 uses the 32-bit graphics port, the data in registers GCKc is used as specified by the PCLK:SCLK ratio.

4.8.2.1 GCKR: Graphics Chroma Key Red

CKR							
7	6	5	4	3	2	1	0

Bit #	Access	Reset	Description	
7:0	R/W	0	CKR	Chroma Key Red.

4.8.2.2 GCKG: Graphics Chroma Key Green

CKG							
7	6	5	4	3	2	1	0

Bit #	Access	Reset	Description	
7:0	R/W	0	CKG	Chroma Key Green.

4.8.2.3 GCKB: Graphics Chroma Key Blue

CKB							
7	6	5	4	3	2	1	0

Bit #	Access	Reset	Description	
7:0	R/W	0	CKB	Chroma Key Blue.

4.6.3 GKMc: Graphics Key Mask

I/O Address	(ISA, MCA Modes)	0x02EC (GKMR: Graphics Key Mask Red)
		0x02ED (GKMG: Graphics Key Mask Green)
		0x02EA (GKMB: Graphics Key Mask Blue)
Base Index Register	(ISA, MCA Modes)	7 (GKMR: Graphics Key Mask Red)
		7 (GKMG: Graphics Key Mask Green)
		7 (GKMB: Graphics Key Mask Blue)
Direct Address	(Coprocessor Mode)	0x1C (GKMR: Graphics Key Mask Red)
		0x1D (GKMG: Graphics Key Mask Green)
		0x1E (GKMB: Graphics Key Mask Blue)

Registers GKMR, GKMG, and GKMB control the Graphics Color Key Mask function.

- When the CL-PX2080 uses the 8 bit VGA port for graphics data, the data in registers GKMc is ANDed with four adjacent graphics pixels. GKMR is compared to the least significant pixel.
- When the CL-PX2080 uses the 32 bit graphics port, the data in registers GKMc is used as specified by the PCLK/SCLK ratio.

4.6.3.1 GKMR: Graphics Key Mask Red

MR							
7	6	5	4	3	2	1	0

Bit #	Access	Reset		Description
7:0	R/W	1	MR	Mask Red

4.6.3.2 GKMG: Graphics Key Mask Green

MG							
7	6	5	4	3	2	1	0

Bit #	Access	Reset		Description
7:0	R/W	1	MG	Mask Green

4.6.3.3 GKMB: Graphics Key Mask Blue

MB							
7	6	5	4	3	2	1	0

Bit #	Access	Reset		Description
7:0	R/W	1	MB	Mask Blue

CL 42021

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4.7 Cursor Positioning

4.7.1 CXb: Cursor X Position

I/O Address	(ISA, MCA Modes)	0x02EC (CXL: Cursor X Position, Low Byte)
		0x02ED (CXH: Cursor X Position, High Byte)
Base Index Register	(ISA, MCA Modes)	3 (CXL: Cursor X Position, Low Byte)
		3 (CXH: Cursor X Position, High Byte)
Direct Address	(Coprocessor Mode)	0x0C (CXL: Cursor X Position, Low Byte)
		0x0D (CXH: Cursor X Position, High Byte)

8 bit registers CXL and CXH specify the X position of the bottom right corner of the cursor relative to the left side of the display screen.

- When CXL = 1 and CXH = 0, the right-most column of pixels of the cursor is positioned at the left most column of pixels of the display screen.
- When CXL = 0 and CXH = 0, the cursor is positioned completely off screen one column to the left of the first displayed column of pixels on the screen.
- During reset, CXH=0x00 and CXL=0x00; the cursor is positioned in the upper left corner off screen.

4.7.1.1 CXL: Cursor X Position, Low Byte

X							
7	6	5	4	3	2	1	0

Bit #	Access	Reset		Description
7:0	R/W	0	X	X position.

4.7.1.2 CXH: Cursor X Position, High Byte

0				X			
7	6	5	4	3	2	1	0

Bit #	Access	Reset		Description
7:4	R/W	0	0	
3:0	R/W	0	X	X position.

4.7.2 CYb Cursor Y Position

I/O Address	(ISA, MCA Modes)	0x02EA (CYL Cursor Y Position, Low Byte)
		0x02EB (CYH Cursor Y Position, High Byte)
Base Index Register	(ISA, MCA Modes)	3 (CYL Cursor Y Position, Low Byte)
		3 (CYH Cursor Y Position, High Byte)
Direct Address	(Coprocessor Mode)	0x0E (CYL Cursor Y Position, Low Byte)
		0x0F (CYH Cursor Y Position, High Byte)

Registers CYb specify the Y position of the bottom right corner of the cursor relative to the top of the display screen.

- When CYL = 1 and CYH = 0, the bottom row of pixels of the cursor is positioned at the top row of pixels of the display screen.
- When CYL = 0 and CYH = 0, the cursor is positioned completely off screen, one column above the first displayed row of pixels on the screen.
- During reset, CYH=0 and CYL =0, the cursor is positioned in the upper left corner off screen.

4.7.2.1 CYL Cursor Y Position, Low Byte

Y							
7	6	5	4	3	2	1	0

Bit #	Access	Reset		Description
7:0	R/W	0	Y	Y position

4.7.2.2 CYH Cursor Y Position, High Byte

0				Y			
7	6	5	4	3	2	1	0

Bit #	Access	Reset		Description
7:4	R/W	0	0	
3:0	R/W	0	Y	Y position

CL 42022

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4.7.3 VFC: Video Format Control

I/O Address	(ISA, MCA Modes)	0x02EC
Base Index Register	(ISA, MCA Modes)	4
Direct Address	(Coprocessor Mode)	0x10

Register VFC sets up the video bus interface timing and color format controls.

RSVD			GE*	CSF			
7	6	5	4	3	2	1	0

Bit #	Access	Reset		Description
7:5	R/W	000	RSVD	Reserved (write as zero).
4	R/W	0	GE*	Gamma Enable. Enables the gamma LUTs.
3:0	R/W	0000	CSF	Color Space Format of Video Bus: 0000 YUV 4:2:2 format Non-tagged data 0001 Y(U:T)(V:T) 4:(2):(2) format (LSB of U and V are Tag data)* 1000 RGB 6:6:6 format 1010 RGB 5:6:5 format 1011 TRGB 1:5:5:5 format (MSB is tag data) 1110 RGB 8:8:8 format Untagged 1111 TRGB 1:8:8:8 format (bit 31 is tag bit) All other bit configurations are reserved.

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4.7.4 SAR: SYNC Alignment Register

I/O Address	(ISA, MCA Modes)	0x02FA
Base Index Register	(ISA, MCA Modes)	4
Direct Address	(Coprocessor Mode)	0x12

Register SAR programs incoming and outgoing sync signals to the monitor in both polarity and PCLK delay relative to the DAC outputs and internal pixel pipeline. This program signals HSIN, HSOUT, VSIN and VSOUT to be active high pulses. SAR also sets the output sync signals VSOUT and HSOUT to align with the DAC R, G, and B outputs in PCLK time units.

HSIP	HSOP	VSIP	VSOP	DLDR	DLY		
7	6	5	4	3	2	1	0

Bit #	Access	Reset		Description
7	R/W	0	HSIP	Horizontal sync Input Polarity 0 HSIN = active low 1 HSIN = active high
6	R/W	0	HSOP	Horizontal sync Output Polarity 0 HSOUT = active low 1 HSOUT = active high
5	R/W	0	VSIP	Vertical sync Input Polarity 0 VSIN = active low 1 VSIN = active high
4	R/W	0	VSOP	Vertical sync Output Polarity 0 VSOUT = active low 1 VSOUT = active high
3	R/W	0	DLDR	Delay Direction of HSOUT, VSOUT relative to R,G, and B 0 Sync Signals behind DAC outputs 1 Sync Signals ahead of DAC outputs
2:0	R/W	000	DLY	Delay in number of PCLKs 000 No delay 111 7 PCLK difference

CL 42023

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4.8 Digital-to-Analog Conversion and Controls

The analog RGB signals produce 0.7 volt peak white amplitude with an IREF of 8.8 mA when driving a doubly terminated 75-ohm load. This process corresponds to an effective DAC output load (R effective) of 37.5 ohms.

The following equation calculates IREF for various peak white voltages and output loading values:

$$IREF = \frac{V_{peak\ white}}{1.097 \times R_{effective}}$$

The following equation applies to all values of IREF and output loading:

$$V_{black\ level} = \text{zero volts}$$

The analog circuitry is powered by the AVDD voltage, which is bonded out separately from the digital power. A decoupling capacitor must be attached externally between AVDD and VSS.

4.8.1 ASC: Analog Setup Control

I/O Address	(ISA, MCA Modes)	0x02FA
Base Index Register	(ISA, MCA Modes)	1
Direct Address	(Coprocessor Mode)	0x08

Register ASC sets up the DAC and analog output.

RSVD	COFF	RSVD				D24	DOFF
7	6	5	4	3	2	1	0

Bit #	Access	Reset		Description
7	R/W	0	RSVD	Reserved (write as zero).
6	R/W	0	COFF	Clock Off 0 Normal operation 1 Powers down the CL-PX2080. Clocks forced high
5:2	R/W	0	RSVD	Reserved (write as zero)
1	R/W	0	D24	18/24-Bit Data 0 18-bit DAC 1 24-bit DAC.
0	R/W	0	DOFF	DAC Off 0 Normal operation 1 Disables the analog circuitry.

4.9 Reserved Registers

I/O Address	(ISA, MCA Modes)	0x02E8 (RSV1 Reserved Register 1)
		0x02EA (RSV2 Reserved Register 2)
		0x02E8 (RSV3 Reserved Register 3)
		0x02EB (RSV4 Reserved Register 4)
Raw Index Register	(ISA, MCA Modes)	4 (RSV1 Reserved Register 1)
		5 (RSV2 Reserved Register 2)
		6 (RSV3 Reserved Register 3)
		7 (RSV4 Reserved Register 4)
Direct Address	(Coprocessor Mode)	0x13 (RSV1 Reserved Register 1)
		0x16 (RSV2 Reserved Register 2)
		0x18 (RSV3 Reserved Register 3)
		0x1F (RSV4 Reserved Register 4)

Registers RSV1, RSV2, RSV3 and RSV4 are reserved.

RSVD							
7	6	5	4	3	2	1	0

Bit #	Access	Reset	Description
7:0	RW	0h	RSVD Reserved (write as zero)

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CL 42024

5. ELECTRICAL SPECIFICATIONS

5.1 Absolute Maximum Ratings

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Storage temperature .... -65°C to +150°C
Voltage on any pin with respect to ground .... -0.5 Volts to Vdd+0.5 Volts
Power Supply Voltage 7V
Lead Temperature (10 seconds) .... 300°C

5.2 CL-PX2080 DC Specifications (Digital)

Symbol	Parameter	MIN	MAX	Units	Conditions
VDD	Power Supply Voltage	4.75	5.25	V	Normal Operation
V_{IL}	Input Low Voltage	0	0.8	V	
V_{IH}	Input High Voltage	2.0	VDD + 0.8	V	
V_{OL}	Output Low Voltage		0.4	V	I_{OL} = 4 mA
V_{OH}	Output High Voltage	2.4		V	I_{OH} = 400 µA
V_{ILC}	Input Low Voltage CMOS		0.8	V	
V_{IHC}	Input High Voltage CMOS	3.0		V	
V_{OLC}	Output Low Voltage CMOS		0.4	V	I_{OLC} = 3.2 mA
V_{OHC}	Output High Voltage CMOS	3.5		V	I_{OHC} = -200 µA
I_{DD}	Digital Supply Current		N/A	mA	V_{DD} Nominal
I_{DDT}	Total Supply Current		N/A	mA	Note 1
I_L	Input Leakage	-10	10	µA	0 < V_{IN} < VDD
C_{IN}	Input Capacitance		10	pF	
C_{OUT}	Output Capacitance		10	pF	

NOTE: 1) I_{DDT} is the sum of I_{DD} + $DACI_{DD}$ + $CLKI_{DD}$. I_{DDT} must be <200mA (package constraint)
2) DACVSS must not exceed V_{DD}.

5.3 CL-PX2080 DC Specifications (RAMDAC)

(VDD = 5V 5%, T_A = 0° to 70C unless otherwise specified)

Symbol	Parameter	MIN	MAX	Units	Conditions
DACVDD	Power Supply Voltage	4.75	5.25	V	Normal Operation
I_{REF}	DAC Reference Current	7.0	10.0	mA	Notes 1, 2
DAC_{IDD}	DAC Supply Current		75	mA	Note 3

NOTE:
1) Reference Current outside the specified limits may cause the analog outputs to become invalid
2) The Dot Clock must be stable for a period of 100 µS after power up before proper DAC operation is guaranteed
3) DAC I_{DD} is specified with the three analog outputs (R,G,B) each loaded with 37.5 ohms

5.4 CL-PX2080 DAC Characteristics

(VDD = 5V 5%, T_A = 0° to 70C unless otherwise specified)

Symbol	Parameter	MIN	MAX	Units	Conditions
R	Resolution	8		bits	
I_{Omax}	Output Current		21	mA	V_O = 1 V
Co	Output Capacitance		12	pF	Blank = V_{IL} MAX
t_D	Analog Output Delay		30	ns	Notes 1,2,3
t_R	Analog Output Rise/Fall time		3	ns	Notes 2,3,4
t_S	Analog Output Settling time		13	ns	Notes 2,3,5
t_{SK}	Analog Output Skew		tbd	ns	Notes 2,3,6
FT	Clock and Data Feedthrough		30	db	Notes 2,3,6
DT	DAC-to-DAC Variability		±2	%	Notes 6,7
GI	Glitch Impulse		75	pV sec	Notes 2,3,6
CT	DAC to DAC Crosstalk		-23	db	Notes 2,3,6

NOTE:
1) t_D is measured from the 50% point of VDCLK to 50% point of full scale transition
2) Load is 37.5 ohms and 30 pF per analog output
3) I_{REF} = -8.8 mA
4) t_R is measured from 10% to 90% full scale
5) t_S is measured from 50% point of full scale transition to output remaining within 2% of final value
6) Outputs loaded identically
7) About the mid point of the distribution of the three DACs measured at full scale deflection

87

CL 42025

May 1991

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5.5 AC Characteristics/Timing Information

This section includes system timing requirements for the CL-PX2080. Timings are provided in nanoseconds (ns) at TTL input levels with the ambient temperature varying from 0 to 70C, and V_{CC} varying from 4.75 to 5.25V DC.

NOTE:
1. All timings assume a load of 50 pF.
2. TTL signals are measured at TTL threshold. CMOS signals are measured at CMOS threshold.

5.5.1 Index of Timing Information

9.9.2 I/O Timing (ISA Bus)

Table 9.1. I/O Timing (ISA Bus)

Symbol	Parameter	MIN	MAX	Unit
t_1	Setup time valid address to IOR*/IOW* active			ns
t_2	Delay IOR*/IOW* active to DEN* active DDIR change			ns
t_3	Delay IOR* active to data out low Z			ns
t_4	Delay IOR* active to data out valid			ns
t_5	Pulse width IOR*/IOW*			ns
t_6	Delay IOR*/IOW* inactive to DEN* inactive DDIR chng			ns
t_7	IOR* inactive to Three State delay			ns
t_8	Address hold time from IOR* IOW* active			ns
t_9	Setup time data valid to IOW* inactive			ns
t_{10}	Hold time IOW* inactive to data invalid			ns
t_{11}	Delay IOW* inactive to next IOW* or IOR* active			ns
t_{12}	Setup AEN rising edge to IOW* or IOR* active			ns
t_{13}	Delay IOW* or IOR* inactive to AEN falling edge			ns

NOTE: 1) AEN must be low.

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CL 42026

NOTE: 2) The low byte address buffer enable must be qualified by IOR* to avoid data contention. See Section 3.1.1 on page 31 for additional information.

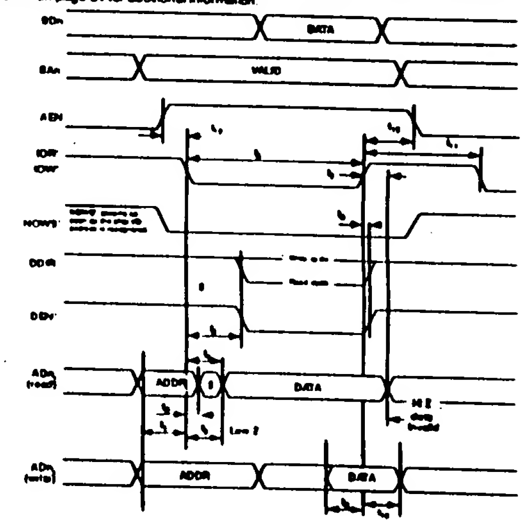

Figure 9-1. I/O Timing, ISA Bus

5.5.2 Timing (MCA Bus)

Table 5-2. CMD' Timing (MCA Bus)

Symbol	Parameter	MIN	MAX	Unit
t_1	Setup time: address valid to CMD' active	80		ns
t_2	Delay CMD' active to DEN' active			
t_3	Status active setup to CMD' active	80		ns
t_4	ADL' active setup to CMD' active	35		ns
t_5	CMD' pulse width	85		ns
t_6	Address hold from CMD' active	25		ns
t_7	Status hold from CMD' active	25		ns

NOTE 1) See Write Cycle and Read Cycle diagrams for data timing with respect to CMD'.

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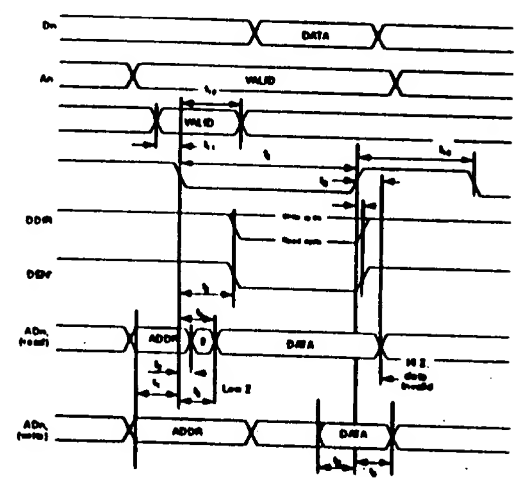
CL 42027

Figure 5-2. CMD' Timing (MCA Bus)



5.5.4 Clocks as Inputs (LCLK = 1:1 Mux Rate)

Table 5-3. Clocks as Inputs (LCLK = 1:1 Mux Rate)

Symbol	Parameter	85 MHz MIN	85 MHz MAX	65 MHz MIN	65 MHz MAX	Unit
t_1	Rise time					
	PCLK0					ns
	PCLK1					ns
	LCLK					ns
	VCLK					ns
t_2	Fall time					
	PCLK0					ns
	PCLK1					ns
	LCLK					ns
	VCLK					ns
t_3	High Period (Note 1)					
	PCLK0	4		8		ns
	PCLK1	4		8		ns
	LCLK					ns
	VCLK	8		8		ns
t_4	Low Period (Note 1)					
	PCLK0	8		8		ns
	PCLK1	4		8		ns
	LCLK					ns
	VCLK	8		8		ns
t_5	Cycle time					
	PCLK0	15		18		ns
	PCLK1	11.6		15		ns
	LCLK	11.6		18		ns
	VCLK	20		20		ns

NOTE 1) LCLK and SCLK cycle and pulse width times are multiplied by 2,4,8 in 2:1, 4:1,8:1 multiplexing modes respectively

88

CL 42028

May 1991

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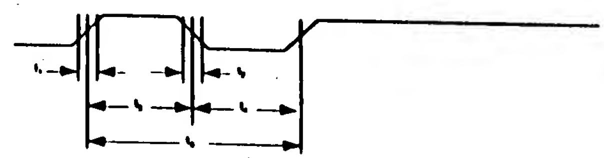

Figure 5-3. Clocks as Inputs

5.5.5 Sync, RGB, and GSD[23:0] as Outputs Delay from PCLKn

Table 5-4. Sync, RGB, and GSD[23:0] as Outputs Delay from PCLKn

Symbol	Parameter	85/65 MHz MIN	85/65 MHz MAX	Unit
t_1	PCLKn rise to R,G,B output delay		30	ns
t_2	R,G,B output rise/fall	3/5		ns
t_3	R,G,B output full scale settling time		13/18	ns
t_4	PCLK rise to VSOUT, HSOUT output delay		10	ns
t_5	PCLK rise to GSD[23:0] output delay		20	ns
not shown				
not shown	R,G,B output to SENSE output delay		1	us

NOTE:
1) Output delay is measured from the 50% point of the rising edge of PCLK to the 50% point of full scale transition.
2) Settling time is measured from the 50% point of full-scale transition to the output remaining within ±1 LSB.
3) Output rise/fall time is measured between the 10% and 90% points of full scale transition.
4) In 1:1 multiplexing mode, RGB data is clocked out directly from LCLK, and synchronizing with SCLK and PCLK is unnecessary and bypassed. All timing PCLK references in table above apply to LCLK when 1:1 multiplexing mode.

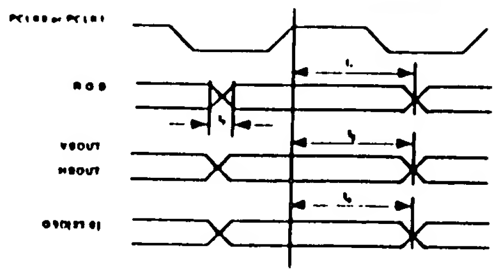

Figure 5-4. Sync, RGB, and OSD[23:0] as Outputs Delay from PCLKn

5.5.8 Graphics Port Interface Timing

Table 5.5 Graphics Port Interface Timing

Symbol	Parameter	85/93 MHz MIN	85/93 MHz MAX	Unit
t_1	LCLK rise to SCLK rise synchronizer setup time	4		ns
t_2	SCLK rise to LCLK rise synchronizer hold time	0		ns
t_3	PCLKn rise to SCLK output delay	10		ns
t_4	Graphics data, control to LCLK rise setup time	4/8	30	ns
t_5	Graphics data, control to LCLK rise setup time	0/2		ns
not shown	R,G,B output full scale settling time		13/15	ns
not shown	R,G,B output to SENSE* output delay		1	us
t_6	PCLK rise to VSOUT,HSOUT output delay	0	10	ns
t_7	PCLK rise to OSD[23:0] output delay	0	20	ns

NOTE: 1)SCLK timing relative to PCLK does not apply when in 1:1 multiplexing mode. In this mode, data is clocked in and out relative to LCLK and no synchronization is performed.

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CL 42029

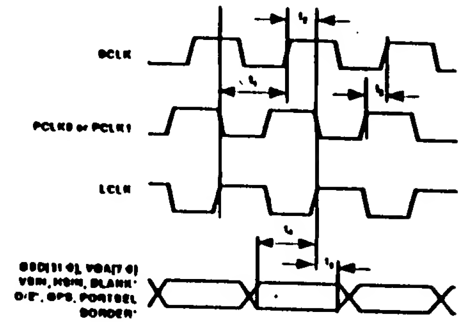

Figure 5-5. Graphics Port Interface Timing.

6 PACKAGE DIMENSIONS — 180 Lead PQFP

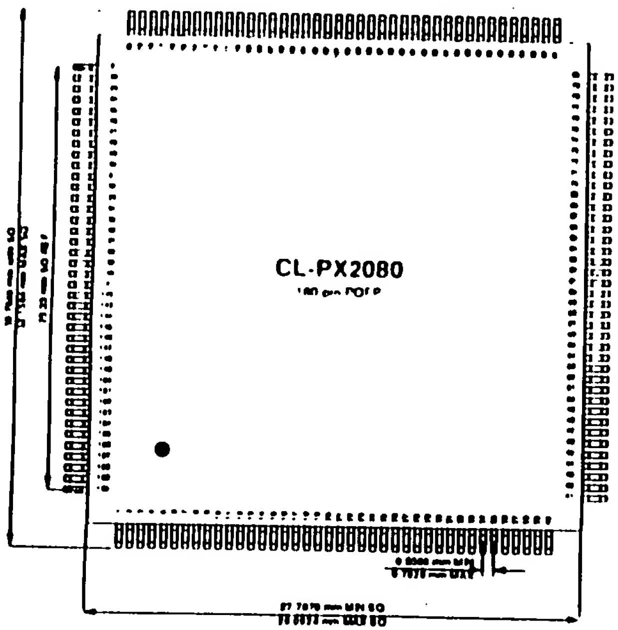

Figure 6-1. CL-PX2080 MediaDAC™ Package Information

CL 42030

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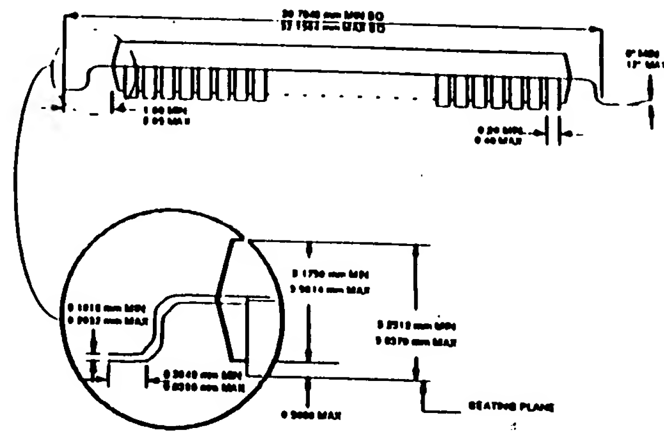

Figure 6-2. CL-PX2080 MediaDAC™ Package Information (Expanded View)

7. ORDERING INFORMATION

When ordering the CL-PX2080, use the following format:

CL - PX 2080 - 65 QC - A

- CL — Cirrus Logic, Inc.
- PX — Product Line: Pixel Semiconductor
- 2080 — Part Number
- 65 — Performance Grade
- Q — Package Type: Q = Plastic Quad Flat Pack (PQFP)
- C — Temperature Range: C = Commercial
- A — Revision[1]

[1] Contact Cirrus Logic for up-to-date information on revisions.

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CL 42031